Low Power High-k Metal Gate
28nm CMOS Solutions for
Mobile High Performance Applications
1. Introduction – The Low Cost, Low Risk Path for 28nm CMOS Manufacturing

High-k Metal Gate (HKMG) is one of the most significant innovations in CMOS fabrication since the inception of silicon VLSI. HKMG enables a revival in transistor scaling that had stalled with poly SiON gate technology, threatening the continuation of Moore’s Law. The Joint Development Alliance and Common Platform Alliance are driving the global standard for High-k Metal Gate (HKMG). Several world-leading semiconductor companies including GLOBALFOUNDRIES, IBM, Intel Mobility Communications (ex-Infineon), Renesas, STMicroelectronics, Samsung Electronics, and Toshiba have participated in the 28nm CMOS Joint Development Alliance. This HKMG solution is far superior to alternatives currently pursued by the other leading foundries, in both scalability (performance, power, die size, design compatibility) and manufacturability. This solution is a “Gate-First” approach that shares the process flow, design flexibility, design elements and benefits of all previous nodes based upon poly SiON gates.

Cost is a substantial advantage of “Gate-First” implementation; a typical foundry customer will save tens of millions of dollars over the course of their 28nm product portfolio life cycle vs. the “Gate-Last” approach due to the 10-20% smaller die size obtainable by “Gate-First.” This presents a tremendous opportunity for customers and for the industry.

“Gate-First” HKMG has already transitioned from the development phase to high volume foundry manufacturing. Notably, AMD has announced production of accelerated processing units (APUs) for laptops and desktop PCs, and CPUs for server applications based on the “Gate-First” technology. This AMD “A-Series” APU is the first foundry HKMG product to ship in the industry. Samsung and ST-Ericsson (see Section 3 below) have also announced wireless products based on “Gate-First” HKMG.
Reduced risk is a hallmark of this low power technology. Lowered risk is realized on several fronts – (1) proven high-volume manufacturing mentioned above, available at multiple Common Platform Alliance locations globally, (2) a fully enabled design ecosystem, with complete design kits available today, (3) sustaining of the industry design style, flexibility and infrastructure utilized at 40nm and all previous technology nodes, (4) superior performance and analog headroom for wider design margin, and (5) lower manufacturing cost. Cost is substantially lower than so-called “High Performance Mobile” solutions from other foundries that require several extra masks to incorporate stress elements to boost performance, and also suffer from the 10-20% die size penalty of “Gate-Last”, as well as from increased area needed for power management implementation to achieve low leakage from a high performance technology.

Table 1 - Risk Reduction offered by 28nm-SLP vs. “Gate-Last” Foundry Offerings

(1) Proven high-volume foundry manufacturing, available at geographically diverse Common Platform Alliance locations that are synchronized for GDS2 compatibility.

(2) A fully enabled design ecosystem, with complete design kits available today.

(3) Sustaining of the industry design style, flexibility and infrastructure utilized at 40nm.

(4) Superior performance and analog headroom (Vcc - Vt) for wider design margin.

(5) Lower manufacturing cost: 20-30% lower than “Gate-Last” “High Performance Mobile” solutions offered by other foundries (much less process complexity and smaller die size).
2. Description of the 28nm Low Power Technology

The low power 28nm process technology is designed for the next generation of smart mobile devices, enabling designs with faster GHz processing speeds, smaller feature sizes, lower standby power and longer battery life. The 28nm process technology is slated to become the foundation for a new generation of portable electronics that are capable of handling streaming video, data, voice, social networking and mobile commerce applications.

28nm Super Low Power (28nm-SLP) is the low power CMOS offering delivered on a bulk silicon substrate for mobile applications. This technology has four Vt’s (high, regular, low, and super low) for design flexibility with multi-channel length capability and offers the ultimate in small die size and low cost. Multiple SRAM bit cells for high density (smallest in the industry) and high performance are available.

The 28nm-SLP is a lower cost technology relative to other 28nm options, being manufactured without the stress elements used to boost carrier mobilities for 28nm poly SiON and for 28nm HKMG HP (high performance) technologies, reducing process complexity and mask count substantially.

3. Superior Mobile Processor Performance up to 2.5GHz with Long Battery Life

In today’s increasingly competitive mobile CPU marketplace, the ability to implement processors for smart portable applications that would enable users to play videos all day or listen to audio for hundreds of hours has been extremely limited. The switch to both HKMG materials and “Gate-First” process architecture have now enabled this to be achieved.
STMicroelectronics, through its wireless JV, ST-Ericsson, is now fulfilling customers’ power and performance demands on the Joint Development Alliance advanced HKMG low power processes. As a case in point, ST is now sampling a dual-core ARM Cortex-A9™ processor that can run at 1.8GHz through the Nova A9540 product. The A9540 is almost 60% faster than previous 45/40nm technology products, while remaining in a battery-powered mobile-power footprint. This technology also benefits the next-generation ARM dual-core Cortex-A15™ CPU which ST-Ericsson will be producing at 2.5GHz in 28nm-SLP, again for smartphone and tablet products, such as the ST-Ericsson Nova A9600 application processor. For product details please see: http://www.stericsson.com/press_releases/NovaThor.jsp.

Another beneficial aspect of this process node is energy efficiency. The “Gate-First” HKMG process enables a functional voltage below 0.8V, which is a first for the mobile industry in an LP process. In fact, the ability for an ARM Cortex-A9™ processor to run at hundreds of MHz and deliver more than 20DMIPS/mW is an industry breakthrough and provides ST-Ericsson a competitive advantage over competing process technologies at the 28nm node.

Figure 1 (next page) shows the scaling in both performance and power of “Gate-First” HKMG vs. the previous generation of 40nm-LP poly SiON. These metrics demonstrate 49% higher frequency, a reduction of 44% in energy per switch per circuit, >25% reduction in leakage power per circuit. The much lower active and leakage power contribute to substantially longer battery life between recharges.

Both transistors are overdriven by 0.1V from their standard operating points. Overdrive is a standard practice by designers that is supported by “Gate-First” HKMG. Overdrive adds flexibility for designers to take advantage of technology to address a wider market spectrum using a single process option (e.g., to cover
both wireless and wired networking applications). Foundry “Gate-Last” offerings are limited in their overdrive capabilities for core transistors or I/O - this is impacting designs which have been using overdrive in past nodes. Thus, overdrive allows both flexibility and further performance gains vs. “Gate-Last.”

Another advantage of 28nm-SLP is the large analog “headroom” (Vcc-Vt) and low noise performance relative to the offerings of other foundries. These electrical factors coupled with the layout advantages cited below in Section 4 combine to offer a far superior analog solution.
4. Smaller Die Size and Lower Chip Cost while Lowering Design Risk and Maintaining Design Compatibility with 40nm

The “Gate-Last” approaches pursued by other foundries are a metal-fill and polish-intensive process which is very sensitive to density and pattern variations. In order to achieve reasonable yield, customer designs must be very regular at the layout level, and thus the foundries have to employ Restrictive Design Rules (RDRs) for “Gate-Last” to force the patterns to be regular. The RDRs impact scaling directly, creating a fundamental impediment to the density doubling, which customers expect as they move to a new technology generation. Figure 2 shows the cell layout and routing advantages of “Gate-First” design rules that allow tighter pitch, dual-orientation poly gates and flexible poly interconnect, in contrast to the single-orientation poly restrictions. In order to mitigate the penalties imposed by these poly restrictions, an additional metal layer must be utilized to prevent the cell from blowing up 10-20% or more.

Figure 2. Dense routing is enabled by “Gate-First” HKMG. Layout schematic shows Metal 1 outlined in brown. Poly interconnect, outlined in white, enables flexible connection and substantially smaller die size of ~10-20% depending on user’s standard-cell library.
Due to compatibility with the conventional poly gate processing flow (as depicted in Figure 2), “Gate-First” enables a reduction in design complexity by preserving design architecture and layout style, thereby leveraging design investments with IP reuse. This design compatibility helps reduce overall risks of adopting 28nm. The RDRs of “Gate-Last” approaches will impose additional new design architecture risks on top of the risk of a leading-edge design, whereas “Gate-First” minimizes any new design architecture risks - leading to faster design turn-around-time. This lowered risk is another big advantage of “Gate-First.”

Specific issues impacting “Gate-Last” analog design include:

- Gate CMP in “Gate-Last” restricts gate length to ≤ 180nm (approx) “Gate-First” does not have this limitation.
  - MOSFET: Allows L >> 180nm for improved analog characteristics, especially Rout and matching.
  - Capacitor: Larger-area capacitors allowed in “Gate-First” lead to higher density than “Gate-Last” with smaller gate-area restriction such as shown in Figure 3.
- The use of conventional poly resistors and poly eFuse in “Gate-Last” technology adds the complexity/cost of additional mask layers.
5. The Super Low Vt Option Extends the Solution for High Performance Wired Applications

The Super Low Vt option also allows a performance boost over the traditional Vt’s available at a given process node. The Super Low Vt option brings >10% performance benefit to the ARM Cortex-A9™ implementation at STMicroelectronics. This opens the door for greater than 2GHz performance. The beauty of the Super Low Vt option is that with just 2 extra masks, and because of design-rule compatibility of standard cells between Super Low Vt and any other standard Vt option, the performance benefit can be realized with a minimum of Super Low Vt cells on the performance critical path. This produces the performance boost with minimal power increase, making this option attractive to applications with specific thermal requirements that still require the largest performance envelope.

Table 2 shows speed and power based on simulations of Cortex-A9™ by GLOBALFOUNDRIES. The Super Low Vt option with overdrive extends the slow corner clock to 1.6GHz, with typical speed of 2.2GHz in a ~0.5W power envelope.

Note that power and performance above are based on SPICE simulation data from GLOBALFOUNDRIES, and are meant to provide an estimate of the technology entitlement of 28nm-SLP. Further details on the core optimization utilized to achieve these results can be obtained from GLOBALFOUNDRIES.

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6. A Rich Design Enablement Solution (ARM and Synopsys) is Deployed and Available Now for 28nm-SLP

The Common Platform Alliance has been collaborating with ARM and Synopsys on the development of a comprehensive 32/28nm System-on-a-Chip (SoCs) design platform using “Gate-First” HKMG technology. ARM has developed an intellectual property (IP) portfolio integrating leading-edge HKMG process technology with ARM advanced microprocessor cores and physical IP including logic, memory and interface products for distribution to their customers. Synopsys has developed a 32/28nm optimized design enablement solution, IP, design tools and methodology optimized for the Alliance’s HKMG technology. Design flows have been proven on multiple test chips.

28nm-SLP ARM standard cell libraries and memory compilers (complete design kits) are available now. Synopsys IP, including multiple standard interfaces (such as USB2.0/3.0, SATA, and PCIe) are also available. Customers can participate on several multi-project wafer reticles annually at Common Platform Alliance fabs.

7. Global Manufacturing – Multiple Fab Synchronization of Critical Parameters for Multi-Site Global Production

GLOBALFOUNDRIES, IBM, Samsung Electronics and ST announced in June 2010 that the four companies are collaborating to synchronize semiconductor manufacturing facilities for the production of advanced chips based on 28nm-SLP. Synchronizing processes involves matching dozens of critical physical and
Figure 4. 32/28nm foundry capacity projection for leading foundries showing greater aggregate capacity for the Common Platform “Gate-First” HKMG vs. the other major foundries. (Market Data estimates by GLOBALFOUNDRIES Strategic Marketing using public data and third party analyst reports).

electrical parameters to help ensure that customers’ chip designs can be produced using a common GDS2 file at multiple sources on three different continents with no redesign required.

The “Gate-First” global alliance presents a global manufacturing capacity and design ecosystem for HKMG that is far greater than the other leading pure-play foundry. Figure 4 shows a capacity projection by an industry analyst.
8. Conclusions

The 28nm low power technology presents tremendous value for the industry in that it meets demanding performance scaling needs from 40nm, and achieves substantially smaller die size than competing foundry offerings. Reduced risk is a hallmark of this low power technology. Lowered risk is realized on several fronts – (1) proven high-volume manufacturing is available at multiple Common Platform Alliance locations globally, (2) a fully enabled design ecosystem with IP and tools and proven design flows, available today, (3) sustaining of the industry design style, flexibility and infrastructure utilized at 40nm and all previous technology nodes, (4) superior performance and analog headroom for wider design margin, and (5) lower manufacturing cost.

9. Acknowledgements

GLOBALFOUNDRIES thanks STMicroelectronics for providing insights into their use of 28nm-SLP for ARM core performance, that ranges from 2.5Ghz under overdrive conditions to functional voltages below 0.8V, which is a first for the mobile industry in an LP process. This enables an industry breakthrough for an ARM Cortex-A9™ processor to run at hundreds of MHz and deliver more than 20DMIPS/mW. For product details, please see http://www.stericsson.com/press_releases/NovaThor.jsp.
About GLOBALFOUNDRIES

GLOBALFOUNDRIES is the world’s first full-service semiconductor foundry with a truly global manufacturing and technology footprint. Launched in March 2009 through a partnership between AMD [NYSE: AMD] and the Advanced Technology Investment Company (ATIC), GLOBALFOUNDRIES provides a unique combination of advanced technology, manufacturing excellence and global operations. With the integration of Chartered in January 2010, GLOBALFOUNDRIES significantly expanded its capacity and ability to provide best-in-class foundry services from mainstream to the leading edge. GLOBALFOUNDRIES is headquartered in Silicon Valley with manufacturing operations in Singapore, Germany, and a new leading-edge fab under construction in Saratoga County, New York. These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, the United States, Germany and the United Kingdom.

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