

FD-SOI Technology Innovations Extend Moore's Law

A GLOBALFOUNDRIES WHITE PAPER

September 2015



Introduction

Fully-depleted silicon-on-insulator, or FD-SOI, is an innovative technology that leverages the established planar process while ensuring a continuation of the efficiency improvements projected by Moore's law. FD-SOI delivers the die size reductions, power reductions, increases in performance and increased functionality projected by Moore's Law without the need to introduce dramatically more complex manufacturing processes. This allows designers and manufacturers to create the truly innovative, break-through products that can make new markets or dominate established ones. FD-SOI is the answer to the often conflicting requirements that challenge designers of low power electronics equipment.



Key Market Trends

Modern electronics systems continue to be dominated by the well entrenched customer expectations of increased performance and growing features, reduced cost and smaller size. Moore's Law has allowed electronics designers and manufacturers to deliver on these expectations for several decades. Recently, energy savings has become a leading market requirement in all market segments and the need for lower power, extended battery operation, and even the use of energy harvesting sources to power electronics systems have grown significantly. Computation efficiency is also a growing concern both on the small and large scale. Compact mobile, Internet of Things sensors and wearables require significant capabilities- often including wireless communications, storage and digital signal processing- but with limited power. FD-SOI minimizes power consumption through the unique ability to optimize for active and standby leakage. This ability extends operating lifetime while also delivering a smaller form factor by reducing heat and using a smaller bill of materials. Also, large server and storage farms with immense power requirements find that computation power efficiency is now the most important element of the cost structure. FD-SOI delivers the unique capability to optimize power efficiency by allowing systems to dynamically adjust power and performance to user demands quickly and easily.

In addition to the market segments described above, other segments are also challenged to deliver on similarly increasing demands. Networking and communications infrastructure are both challenged to deliver the increased bandwidth needed to implement cloud based systems and to deliver higher resolution media content desired by increasingly mobile consumers. The industrial market will also see an explosion in sensor use to further automate, track and control industrial processes, optimize processes and manage material transport to reduce energy use and cut costs. Implementing the increased processing required, without increasing power consumption, is necessary for the successful deployment of the Industrial Internet of Things.

Recent challenges to the continued applicability of Moore's Law has brought into question if these established customer expectations can continue to be met. An innovative process that uses established manufacturing techniques while extending Moore's Law is critically needed.



An Introduction to FD-SOI Technology

Fully depleted silicon on insulator (FD-SOI) technology is a planar process that leverages existing manufacturing methods to deliver reduced silicon geometries, improved performance and low power. This extends Moore's Law without the need for significantly more complicated manufacturing processes. Two key innovations are combined, synergistically, to create the FD-SOI process. The first is the use of an ultra thin oxide insulator placed on the top of the base silicon. Second, a very thin silicon layer creates the transistor channel. Due to the thinness of this layer, no channel doping is required, making the transistor fully depleted. The resulting FD-SOI structure is an evolution from the familiar bulk CMOS process, as shown in the illustration in *Figure 1*.

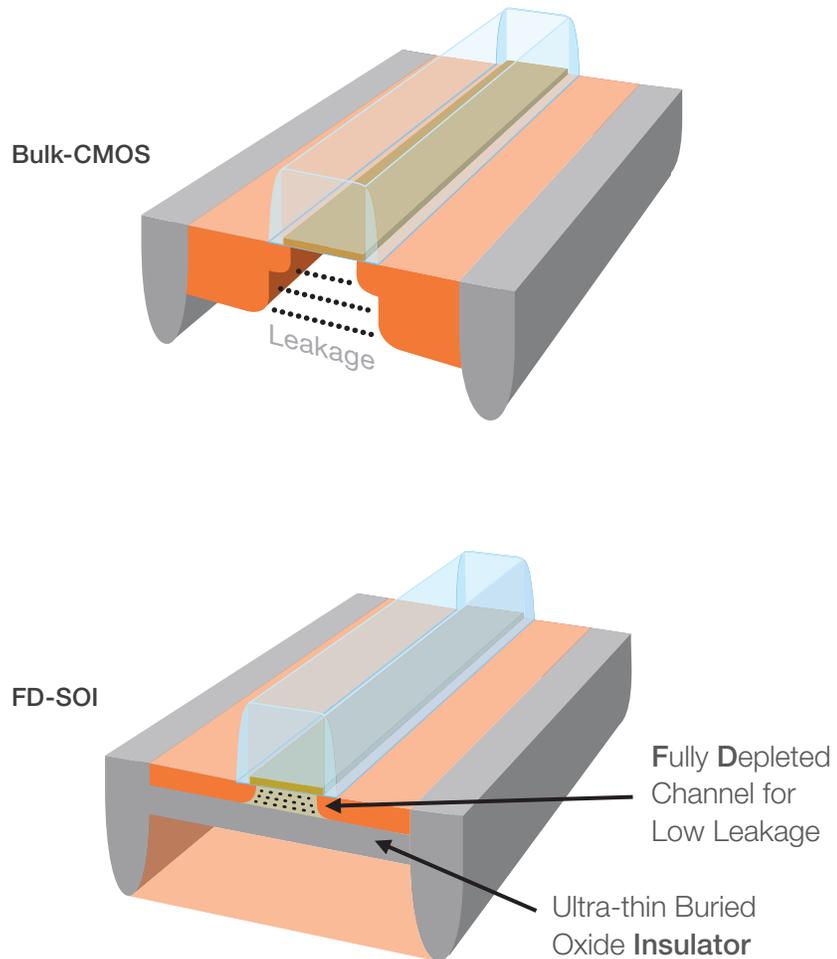


Figure 1: FD-SOI Transistor Structure Compared to Bulk CMOS

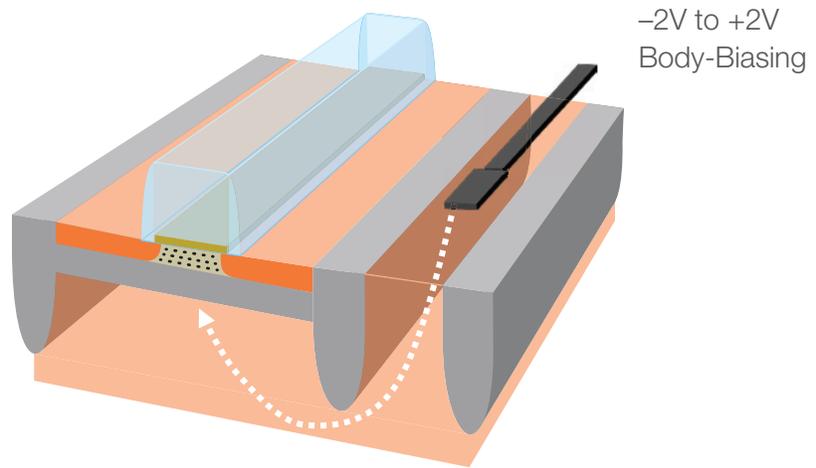
Advantages of FD-SOI Technology

The FD-SOI structure results in much better transistor characteristics compared to traditional bulk CMOS technology. As illustrated in *Figure 1*, the FD-SOI buried oxide layer reduces the parasitic capacitance between the source and drain exhibited by bulk technology. The buried oxide layer also constrains electrons flowing between the source and drain to significantly reduce performance- and power-degrading leakage currents. The fully depleted channel also reduces leakage.

FD-SOI technology allows control of the transistors' behavior not only through the gate, but also by applying a voltage, often called biasing, to the substrate underneath the device. Body biasing is very limited when used in bulk technology due to parasitic current leakage and inefficiency at reduced transistor geometry. In FD-SOI technology, biasing is much more efficient due to the dielectric isolation created by the buried oxide layer. Additionally, the isolating properties of the buried oxide layer allow the use of higher biasing voltages, resulting in innovative dynamic transistor control to select between speed and power efficiency. These advantages translate to a 20% lower die cost and a 50% lower mask cost than more complicated processes such as FinFET. Applying the body-bias results in even larger performance and power improvements.

As shown in *Figure 2* below, when applying Forward Body Biasing, or FBB, less voltage is required on the gate to switch the transistor, resulting in faster transistor switching with less active power consumption. This is ideal for circuits that need to minimize energy consumption while operating. When the same circuit is operated in a standby mode, it is desirable to not apply FBB. This will result in slower transistor performance, but at a lower leakage power level. FBB can be easily changed dynamically to switch a group of transistors to a higher performance higher power mode from a normal operation mode or to a lower performance lower power mode from a normal operation mode. In a similar manner, Reverse Body-Biasing can also be utilized in FD-SOI. Applying RBB means that more voltage needs to be applied to the gate to switch the transistor. This mode is ideal for circuits that are often in standby mode and require extremely low off-state leakage. Optimizing circuits to use FBB and RBB allows designers to select circuits for faster or more efficient operation when high speed is required and lower leakage power when performance isn't as critical.

Figure 2: Efficient Body Biasing for Selectable Lower Power or Improved Performance



Combining the body-biasing knobs with common techniques used for power management in bulk technologies gives the designer additional flexibility. FD-SOI provides multiple knobs for V_t 'mixing' for optimizing leakage and timing in a design. V_t types are determined by the back-gate dopant, the channel implant, and the gate-length size. Combining body-bias with Dynamic Voltage and Frequency Scaling (DVFS) techniques provides the designer the ability to optimize for dynamic and static leakages.

Advantages of FD-SOI Technology for Common Circuit Blocks

The key advantages of FD-SOI technology are perhaps best illustrated by looking at the impact FD-SOI has on several of the most common circuit blocks used in electronics devices.

Digital Logic Blocks

In digital logic blocks increased power efficiency is perhaps the most important requirement. Increasing performance and adding more functions without going over a power budget is the continuous evolution of digital systems. FD-SOI technology delivers a reduction in capacitance associated with the transistors used in digital circuits, delivering faster and more efficient switching which results in improved performance and reduced power. Additionally, the ability to dynamically adjust the bias voltage allows increased flexibility in applying power to where it can be used most efficiently, a true innovation for managing power efficiently. A reduction in leakage current also helps improve static power dissipation, which can be a concern in large digital logic blocks.

Analog and RF Blocks

In analog blocks, FD-SOI technology delivers several advantages that can dramatically differentiate device characteristics. The total dielectric isolation of the channel creates lower gate capacitance and reduced leakage currents. Isolation also provides latch-up immunity so smaller and simpler analog circuits can be used. Additionally, the absence of channel doping and pocket implants in the fully depleted transistor produce lower noise specifications and higher gains when compared to bulk technologies - key differentiators in advanced analog systems. FD-SOI also improves RF block characteristics with very high f_T , f_{Max} and flat behavior, as well as flat and high g_M results. These key characteristics result in best in class RF and analog designs.



Embedded SRAM

As the need for embedded SRAM cells that span the full range from HD to ULV increases, the requirements for successful implementations become more stringent. Power efficiency, for example, becomes a more critical requirement and reductions in both static and dynamic power dissipation are needed to improve efficiency. The very low leakage current of FD-SOI technology provides dramatic improvements in static current for large SRAM blocks without negatively impacting performance. The ability to dynamically adjust bias voltages, perhaps on a block basis, can deliver large improvements in dynamic current as well. Reduced gate capacitance means that smaller row drivers can be used and this also improves dynamic current requirements. Finally, the low voltage operation provided by FD-SOI directly reduces overall power dissipation for the entire SRAM block. FD-SOI technology also enables smaller SRAM cell size and provides a significant die area reduction. SRAM reliability is also increased when using FD-SOI when single event upset (SEU) events are considered. FD-SOI can also implement cells across the full range from HD to ULV to address the widest range of embedded applications as possible.



A Robust Future for FD-SOI Technology

The FD-SOI process is an important evolutionary step from the familiar bulk CMOS process and can leverage much of the design tools, manufacturing infrastructure, and IP ecosystem already in place. In fact, the transition from 55/40/28nm technologies to 22nm FD-SOI is very straightforward in terms of design enablement, and EDA tools support. This speeds time to market and minimizes start-up time and the investment associated with more drastic process changes, like that associated with a 16nm non-FD-SOI technology. The process is expected to scale to the 10nm node, so it also has a very robust future.

Conclusion

FD-SOI is a breakthrough technology with a robust future. It extends Moore's Law to allow the creation of differentiated capabilities that provide increased value to end customers. To find out more visit the GLOBALFOUNDRIES FD-SOI web page at globalfoundries.com/22fdx.



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