

55LPx

55 nm Process Technology

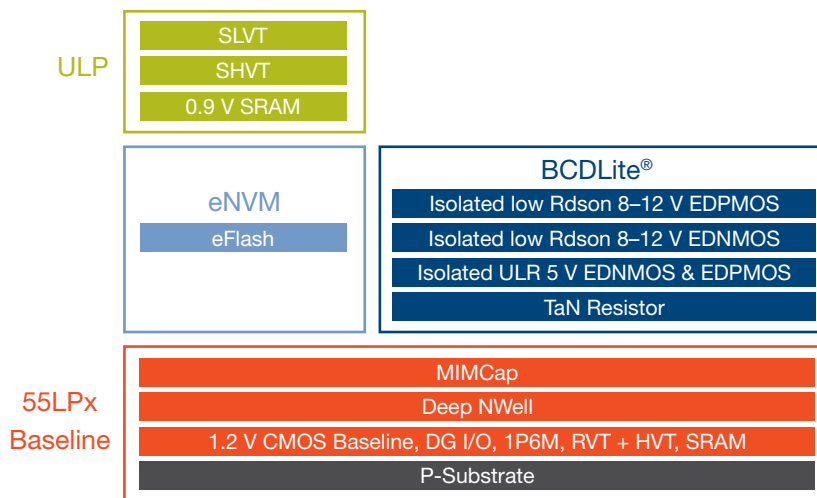
Highlights

- Single 55 nm platform with one model and PDK and IP re-usability for maximum ROI
 - + Manufactured in Singapore
 - + High volume production capability with world-class D0 (<0.04 def/in²) defect density
- Optimized for integrated analog, power and mixed-signal applications
 - + Consumer and Industrial
 - + IoT and Wearables
 - + Automotive MCU
 - + Low to mid-range MCUs
 - + HV (DDI/TDDI) and Analog
- Comprehensive design ecosystem
 - + Full range of Foundation and Complex IP libraries
 - + PDK and reference flows supported by major EDA and IP partners
 - + Proven eNVM technology with high endurance and high reliability
- Extensive services and supply chain support
 - + Regularly scheduled MPWs
 - + Layout database consolidation and mask assembly services
 - + Advanced packaging and test solutions including 2.5D and 3D

Enabling *Connected Intelligence*

GLOBALFOUNDRIES 55LPx process technology platform enables IP reusability across multiple applications in both Consumer and Automotive markets, optimizing resources, reducing cost and improving time-to-market.

The comprehensive, highly configurable and production proven 55LPx platform solution enables integration of logic, RF, analog and non-volatile memory to provide cost effective solutions.



Target Applications and Solutions

- Automotive (body electronics / power train) (55LPx+eNVM)
- Secure applications (Smart Cards, card reader) (55LPx+eNVM+RF)
- Battery-powered, next-generation SoC (Wearables) (55LPx+eNVM+RF+ULP)
- Battery-powered IoT end nodes (55LPx+eNVM+RF+ULP)
- Smart Energy/Grid (Smart meters) (55LPx+eNVM+RF+ULP)

Technology Overview

- 55 nm LPx with 1.2 V and 2.5 V CMOS logic
- 5 V EDMOS, APMOM, MIM
- 55 nm BCDLite® with 8–12 V and ULR 5 V EDMOS and EDPMOS, TaN Resistors
- 55 nm ULP with SLVT, SHVT, 0.9 V SRAM and 0.9 V standard cell library with Always-on blocks
- eNVM 0.09 μm^2 eFlash bit cell, Automotive Grade 1
- Operating temperature range: -40°C to 125°C

IP Overview

The 55LPx Platform IP portfolio includes a wide range of silicon-proven high performance, power-optimized solutions for a broad set of applications.

Foundation IP

Standard Cell 2.5/1.2/0.9 V (8T, 9T, 12T)	
SRAM & ROM Compiler	GPIO
Analog and Digital PLL	Always-on Std Cells

Interface IP

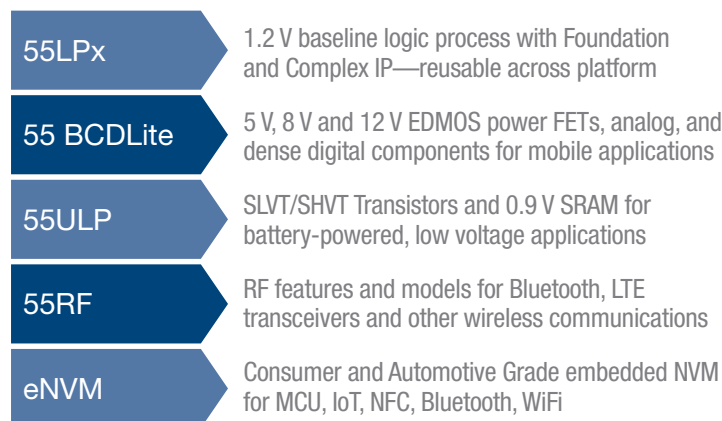
DDR3/2	LPDDR3/2	HDMI 1.4
MIPI D-PHY	PCIe G1/2	USB3.0/2.0
SATA I/II		

Memory

NVM: eFlash	NVM: eFuse	NVM: OTP
ROM	SRAM	

Contact GF for IP availability.

55 nm Platform Extensions



55 nm High Performance and High Reliability eFlash solution



Fast Speed

- Read Access $\sim 8\text{--}10$ ns
- Sector Erase time $\sim 2\text{--}3$ ms
- Word Program speed ~ 5 μs

Small Macro

- 0.0904 μm^2 bit cell
- Optimized macro
- Flexible macro form factor

Cost Benefit

- 2x die per wafer in 55 nm compared to 90 nm

High Density

- NVM Memory density up to 16 Mb

Power Efficient

- 55 nm ULP
- Active $I_{\text{Read}} < 100$ $\mu\text{A}/\text{MHz}$ (low-power mode)

Reliable

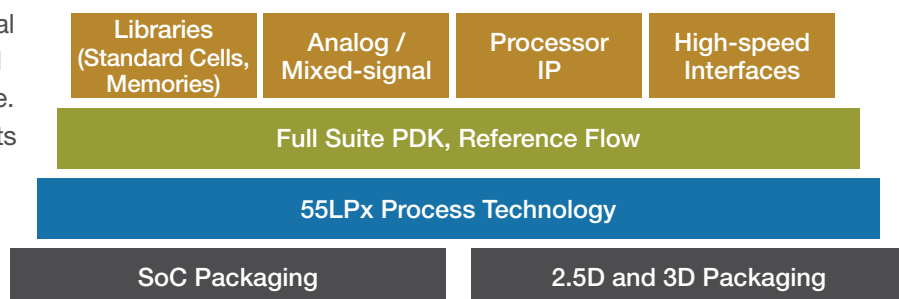
- Automotive grade
- 20 year data retention

Endurance

- $>500\text{k}$ Cycles

GLOBALSOLUTIONS® Design and Manufacturing Ecosystem

GLOBALSOLUTIONS is the sum of our internal resources and ecosystem partners, combined to efficiently enable the fastest time-to-volume. This ecosystem includes partners in all aspects of design enablement and turnkey services, OPC and mask operations, and advanced capabilities in assembly solutions.



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