



GLOBALFOUNDRIES®

Cu-32

Boost performance in chips for networking and cloud hardware with HKMG SOI ASIC



Highlights

- Achieve higher system level throughput with high-k metal gate SOI technology
- Differentiate your design with intellectual property designed to help you achieve higher bandwidth, faster data transmission and packet processing, more on-chip data storage and optimized SoCs
- Access packaging innovations to boost performance
- Tune your design to meet power, performance and area targets with a comprehensive design methodology

It's never ending. The communications infrastructure must continually evolve to stay ahead of exponentially growing numbers of connected devices and skyrocketing volumes of data traffic. Semiconductor solutions targeted for this space must deliver more performance, better power efficiency and added function in less circuit area. Gaining and sustaining a competitive advantage in this environment means implementing advanced semiconductor technology that offers clear differentiation and delivers predictable results. GLOBALFOUNDRIES' 32nm ASIC offering, Cu-32, is designed to help you meet all these challenges.

Achieve higher throughput at system level

The Cu-32 design system takes advantage of silicon-on-insulator (SOI), high-k metal gate (HKMG) technology. The technology is optimized to help you achieve higher levels of performance, power efficiency and integration in your designs for faster throughput at the system level. For example, compared with 45nm SOI technology, our HKMG SOI technology offers:

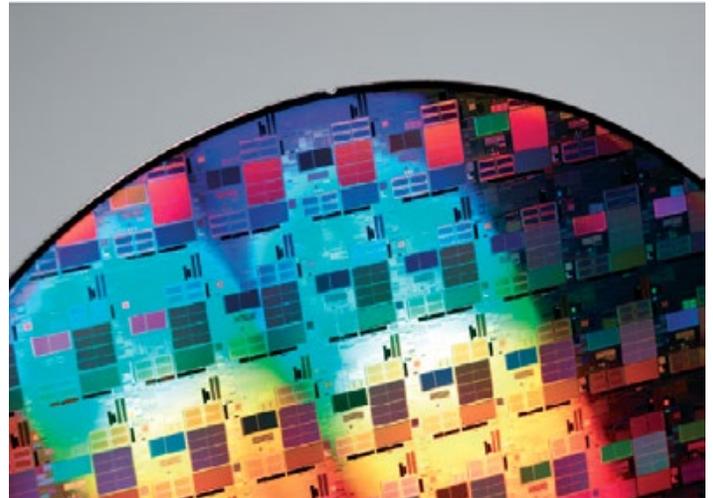
- Up to 25 percent improvement in chip performance
- Up to 30 percent lower power
- Up to 50 percent area savings for logic and memory

Cu-32 enables you to draw on the company's leadership in developing and manufacturing advanced semiconductor technology. You can leverage a proven technology platform designed to meet the demands of next-gen solutions for smarter communications—today.

Differentiate your silicon

Designed to deliver concrete differentiation, the Cu-32 intellectual property portfolio features advanced embedded memories, high-speed SERDES (HSS) cores and a broad range of embedded processor options:

- **Trench-capacitor-based eDRAMs.** Innovative eDRAM technology delivers high performance, low power and the ability to integrate more than one gigabit of on-chip memory in SoC designs. The company's eDRAMs feature significantly lower soft error rates than eSRAM alternatives, and can provide up to a 3x density improvement and up to a 20x reduction in leakage power compared to eSRAMs. More than 3,000 configurations are possible with the Cu-32 eDRAM compiler.
- **High performance, low power ternary CAMs (TCAMs).** Cu-32 features one of the industry's fastest, lowest-power ternary TCAMs to accelerate data lookups in 4G network and cloud hardware.
- **HSS cores.** Cu-32 HSS cores deliver superior jitter performance and equalization across a wide range of interface standards. Cu-32 HSS offerings take advantage of cutting-edge packaging materials to speed network and cloud data transmission and include an advanced 28G backplane core.
- **Microprocessors.** The Cu-32 embedded processor lineup is designed to help clients optimize performance, power efficiency, scalability and value in SoC designs. It includes 32-bit microprocessors and peripherals licensed from ARM and Synopsys along with solutions built on IBM Power Architecture® technology.



Cu-32 wafer

Additional IP building blocks and design enablement resources are available directly and through third party suppliers.

Boost performance with unique packaging architectures

Packaging solutions for Cu-32 are designed to boost performance beyond silicon scaling alone and benefit from pioneering research, close collaboration with industry leaders and integration of advanced materials. The Cu-32 packaging portfolio comprises a wide range of options that take advantage of concurrent silicon/package design, which enables an optimized system solution supporting high link rates and density.

Cu-32 at a glance

| | |
|----------------------------|--|
| Process generation (nm) | 32 |
| Technology | SOI HKMG |
| Supply voltage (VDD) | 0.9 V/0.85 V |
| Wireable gates (millions) | ~400 |
| Total levels of metal | 11 |
| Multi-Vt design libraries | Regular Vt, mezzanine Vt, ultra-high Vt |
| Memory compilers | <ul style="list-style-type: none"> • Fast Trc eDRAM (SRAM alternative) • Multi-banked eDRAM (bandwidth optimized) • Pseudo two-port eDRAM • Ternary CAM • Dense one- and two-port SRAMs • Dual-port SRAM • Low leakage single-port SRAM • High performance single-port SRAM • Two- and four-port register arrays • Low leakage single-port register array • ROM • One-port and dense two-port register files |
| HSS | <ul style="list-style-type: none"> • 28G backplane core supporting 32G Fibre Channel and 100G Ethernet over Copper standards • PCI-Express Gen3 core supporting PCI-Express Gen1, Gen2 and Gen3 standards • 15G backplane core supporting 16G Fibre Channel standard • 15G chip-to-chip core supporting low-power optical and chip-to-chip applications • 6G standards core supporting PCI-Express Gen1 and Gen2 standards |
| 32-bit embedded processors | <ul style="list-style-type: none"> • ARM Cortex-R4, Cortex-A15, Cortex-A12/A17, Cortex-A7 and Cortex-M4 processors; Mali-450 GPU; CoreSight and CoreLink peripherals • Synopsys ARC processors • IBM PowerPC® 4xx cores and IBM CoreConnect™ bus architecture |
| Advanced packaging | <ul style="list-style-type: none"> • High performance substrate build-up materials that can enable 60% longer 28G HSS nets compared to other technologies • System-in-package configurations that include heterogeneous integration of ASIC and foundry technologies and/or custom off-the-shelf components • 2.5D and 3D die stacking architecture that enables mixing and matching of logic, memory and technology nodes for more functional density, lower power and higher performance (semi-custom)* • Low-cost, coreless carriers |
| Power management options | <p>Base:</p> <ul style="list-style-type: none"> • Multi-Vt design libraries (trade off power and performance) • Clock gating (by design or through synthesis) • Power supply flexibility (IP in voltage islands can use different supply voltages) • Selective voltage binning • Low-power SRAMs • Memory power gating <hr/> <p>Semi-custom:*</p> <ul style="list-style-type: none"> • Voltage island power gating (turn off unused areas of a chip) <hr/> <p>Full custom:†</p> <ul style="list-style-type: none"> • Dynamic voltage scaling (modify power supply on-demand, with feedback) • Dynamic frequency scaling (modify clock on-demand, with feedback) |

Optimize power, performance and area

GLOBALFOUNDRIES design methodology uses a holistic, system-level design approach. The methodology features statistical timing and innovative power-management approaches:

- Statistical timing accounts for product aging, environmental and manufacturing process variations, and then models the sensitivities of these variations, along with the individual processing steps and the tracking between them. This in-depth analysis reduces pessimism in timing results to help prevent potential “overdesign” and enables you to tune your design for added power, performance and area advantages. And because statistical timing requires only two functional corners, fewer timing sign-off runs are needed, which can help reduce turnaround time.
- Our design methodology handles both voltage and temperature as variables, which enables designers to develop highly optimized chips that meet system-level power targets. The methodology is designed to streamline implementation of our innovations in power management, including:
 - Voltage islands, which enable power supply flexibility and granular on/off control
 - Patented selective voltage binning, which enables adjustment of on-die voltage as a function of semiconductor process, resulting in chip designs that burn only as much power as needed to meet frequency objectives

For more information

To learn more about Cu-32, contact your sales representative or visit: globalfoundries.com

*Semi-custom: base methodology is provided as part of the ASIC methodology, customization is needed to support each product.

†Full custom: developed on a product by product basis.

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