65nm and 55nm LPe-RF Foundry Technologies

Overview

GLOBALFOUNDRIES 65nm and 55nm RFCMOS technologies offer cost-effective solutions to address the most challenging wireless RFSoC applications. Built on the company's low power enhanced (LPe) platform, the 65nm and 55nm RFCMOS technologies combine the benefits of a rich baseline logic technology and IP ecosystem with world-class RF features and PDKs, enabling a seamless transition to digital logic SoCs with higher levels of RF integration. Examples of 65nm/55nm RFCMOS applications produced in high volume at GLOBALFOUNDRIES include:

- Bluetooth
- GPS
- LTE transceivers
- Digital TV tuners/demodulators
- WiFi/BT/GPS/FM combo SoCs.

RF-specific Features

Using a multi-Vt baseline logic process, the 65nm and 55nm LPe-RF technologies add RF-specific features such as:

- Deep n-well devices
- LDMOS/EDMOS FETs
- Parasitic bipolar devices
- MOS/HA varactors
- Precision resistors
- MIMcaps/MOMcaps
- Inductors
- Thick metals

These features enable you to achieve the performance and integration level required by the most demanding wireless applications. Device mismatch modeling, ESD kit enablement, statistical and corners modeling and DFM features ensure your design is robust and ready for high volume manufacturing.

Robust PDKs

PDK enablement is an integral part of RF design, and our 65nm and 55nm RFCMOS technologies contain specific EDA features that are critical to maximizing first-time-right success in RF. The PDKs are built upon layout-optimized scalable devices with hardware-correlated RF SPICE models. The models are further enhanced by precise parasitic extraction models to account for layout-specific impairments which affect RF performance.

Also, we partner with the leading providers in EDA, IP, prototyping and design services who are recognized for helping to accelerate customer time-to-market with reduced manufacturing risk.

A Complete Foundry Platform for RF Design

Silicon Process

- f_T : 164–185GHz
- Low-power CMOS
- Collaborative process development
- Marketplace success & maturity – Mobility & Connectivity SoCs, LTE radios, GPS, Wi-Fi, Bluetooth, DTV and more

RF Models

- Silicon-validated RF Models
- Layout-optimized RF devices
- Process and corner modeling
- Device noise modeling – Monte-Carlo & Statistical

Design Enablement

- Devices – FETs, Resistors, MOM/MIM caps, UTM. DNWell, LDMOS, EDMOS
- Layout – ESD kit, DRC/LVS/PEX
- Advanced RF simulation capability - EMX, HFSS, Momentum

Technical Support

- Regional field technical support
- Collaborative IP development through partnerships (ex. Catena, ChipIdea)
- GlobalShuttle MPW Program
- MOSIS MPW program

RF TECHNOLOGY PLATFORM

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Baseline Features

Feature	Technology Node
	55nm LPe, 65nm LPe
Core Vdd (V)	1.2
I/O Voltage Options (V)	1.8 / 2.5 / 3.3
Multiple Vt Options	LVt, RVt, HVt
Metallization	Cu , low K
Resistor Options	Nwell, Diff Rs, Sal Poly, UnSal Poly, precision poly resistor
Capacitor Options	APMOM, MIM & MOS Caps
Varactor Options	MOS, Hyperabrupt*
EDMOS	5V and 5V-iso*
VPNP/VNPN	Yes
Thick top metal	3µm Cu
28K Al Cap layer	Yes
eFuse	Yes

RF Features

Device	Parameter	55nm Features	65nm Features
SG NFET, PFET	Peak f_T	185, 100GHz	164, 90GHz
DG NFET, PFET	Peak f_T	36, 22GHz	35, 20GHz
SG NFET	NF_{min} (dB) @ 5GHz & Vg=Vd=Vdd	0.22	
N+ Diffusion Resistor	Sheet Resistance, Tolerance	115.5Ω/□, +/-20%	
P+ Poly Resistor	Sheet Resistance, Tolerance	700Ω/□, +/-15%	
Nwell Resistor	Sheet Resistance, Tolerance	550Ω/□, +/-25%	590Ω/□, +/-25%
Precision Resistor*	Sheet Resistance, Tolerance	370Ω/□, +/-10%	
Inductor (3um Cu + LB Termination)	Q_{peak} @ 0.43nH	21.93	
MOS Var (NCAP)	Capacitance Density (accumulation)	44.6 f F/µm^2	
	Tuning Range (Cacc/Cmin)	6.2	
VNCap	Density (5Mx levels), Tolerance	2.25 f F/µm^2, +/-20%	
APMOM Cap	Density (5Mx levels), Tolerance	2.69 f F/µm^2,+/-15%	
MIM cap – Nitride*	Density, Tolerance	2.2 f F/µm^2. +/-15%	2.25 f F/µm^2. +/-15%

* optional device