FX-14™ Tapeouts Using GF ASIC Design Methodology
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Company Highlights

**REVENUE**

- Approx. $6B* Revenue

**MORE THAN**

- 25,000 Patents & Applications
- 250 Customers
- 18,000 Employees

**FAB LOCATIONS**

- Burlington
- East Fishkill
- Dresden
- Malta
- Singapore

**FAB CAPACITY**

- 300mm Trusted Foundry
- 200mm 200K Wafers/Mo
- 200mm 133K Wafers/Mo

*Based upon analysts' estimates
Global Manufacturing Capacity: ~7M Wafers/Yr*

- **East Fishkill, New York**: 14,000 (300mm)
- **Malta, New York**: Up to 60,000 (300mm)
- **Burlington, Vermont**: 40,000 (200mm)
- **Dresden, Germany**: 60,000 (300mm)
- **Singapore**: 68,000 (300mm), 93,000 (200mm)

**TECHNOLOGY**
- 90nm–22nm
- 28nm, ≤ 14nm
- 350nm–90nm
- 45nm–22nm
- 180nm–40nm

**CAPACITY IN WAFERS/MONTH**
- 14,000 (300mm)
- Up to 60,000 (300mm)
- 40,000 (200mm)
- 60,000 (300mm)
- 68,000 (300mm), 93,000 (200mm)

*200mm Equivalents*
IBM ASIC Business Model (pre-divestiture)

- 20+ years producing first-time-right silicon
- Significant player in the ASIC market
  - Limited fab volume
  - Bulk of customers in wired/wireless networking space
- Netlist handoff or turnkey or services
  - Usually a netlist handoff
  - Sometimes a joint or customer-owned Place/Route
- Test insertion/verification
  - Test insertion RC, then Encounter Test
- Place/Route
  - using IBM EDA tools
- Timing Signoff
  - using IBM EDA tools
  - customer delivers signoff constraints in IBM EinsTimer™ format
IBM ASIC Methodology (pre-divestiture)

• Utilize IBM technologies
  – 14nm SOI in 2013 timeframe
• Interaction with IBM Server
  – Commonality where possible
  – ASIC more flexible than Server
• Heavy dependence upon internal IBM EDA tools
  – Synthesis (limited)
  – Place and Route
  – Timing signoff
• Commercial tool usage in Synthesis, Simulation, Test, and Physical Verification
• Packaged into a robust IBM GUI application, built on flows defined in XML
IBM ASIC Design Phases (RTx)

• RTA: Release To Analysis
  – Early netlist drop, what-if analysis

• RTF: Release To Floorplanning
  – Partially complete netlist, begin detailed floorplanning
  – Exercise placement, cts, routing in an experimental fashion

• RTP: Release To Preliminary
  – Mostly complete netlist, longest phase
  – Complete all steps needed for tapeout (at reduced quality)

• RTL: Release To Layout
  – Final netlist, use learning from RTP to produce a tapeout ready design

• RTC: Release To Checking
  – Submit the shapes to the process engineering team for final assembly
Divestiture to GLOBALFOUNDRIES

- Announced in October 2014, completed in July 2015
- Transition away from IBM EDA tools
  - Reduce dependency upon IBM EDA
  - Utilize improvements found in commercial tools
  - Some Cadence RC/EDI experience from 45/32/14nm
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<td>Tapeout Experiences</td>
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FX-14™ ASIC Builds on Continued Industry Leadership

Decades of experience partnering with industry leaders to enable network transformation

11 consecutive years as top ASIC supplier for wired communications*

Successfully enabled, designed & released some of industry’s most complex ASICs

Outstanding record of enabling first-pass design success

Access to industry-leading experts for continued pipeline of innovation

*Gartner, 2004-2015; includes IBM Microelectronics rankings.
FX-14™ ASIC Offering

Design system is available now

**Intellectual Property**
64-bit & 32-bit ARM® cores, 56G SERDES, world-class embedded TCAM & SRAM

**Technology**
Cost-effective, leading-edge 14LPP technology for differentiated performance, power & area

**Scale**
High-capacity, state-of-the-art semiconductor manufacturing facility

**Design Enablement**
Industry-standard EDA tool suite and proven, best-in-class design methodology
GF ASIC Business Model

- Utilize proven Test/Timing experience for first-time-right silicon
- Significant player in the ASIC market
  - Increased fab volume (order of magnitude)
  - Broader scope and customer base going forward
- Netlist handoff or turnkey or services
  - Broader focus for ASIC, COT services, etc
  - Same RTx design phases for “typical” ASIC designs
- Test insertion/verification
  - using RC/Genus 15.2, Encounter Test 15.1
- Place/Route
  - using Innovus 15.2
- Timing Signoff
  - using Tempus 15.2
GF ASIC Methodology

• Utilize GF technologies
  – e.g., FX-14™

• Commercial tools

• Methodology add-ons (“secret sauce”)
  – Test
  – Clocking
  – Timing signoff
  – Place and Route

• Wrapped in GF framework

• Several tapeouts and in-flight designs
1. IBM ASIC
2. GF ASIC
3. GF ASIC Design Methodology
4. Tapeout Experiences
Full transition to commercial tools

- RC/Genus
  - test insertion
  - synthesis (internal)
- Innovus Place/Route
  - Transitioned from EDI in July 2015
- Quantus Extraction
- Tempus Timing
  - Including TSO
- Encounter Test
  - no change
- Voltus
- Conformal
- NCsim
  - no change
GF Methodology Framework (dflow)

- GF ASIC team is multi-disciplined using various tools and flows
  - Hundreds of designers from PnR, Timing, Test, IP, Physical Verification, etc
  - Converge on a single, light-weight framework that works for everyone (tool agnostic)
- Develop in-house solution
  - Least cost, most flexible, easiest to support
  - Built initial PnR flow using Foundation Flow Tcl as a guide
- dflow = “Design Flow”
  - Flexible control interface (parms) and extensible architecture
  - Local or batch submission
  - Consistent log, netlist, report management
  - Robust Tcl API to support a variety of EDA tools
  - Built-in design data analytics (see later slide)
  - No GUI, robust script interface for highest productivity
GF Methodology Framework (dflow)

- dflow (perl)
- methodology recipe (tcl)
- GF Tcl API
- EDA tool

GF Methodology
Design Team
EDA vendor
GF Methodology Framework (dflow)

dfconfig.tcl parms

def::parm project.name 'ChipX'
def::parm tech.name 'fxt4'
def::parm tech.version 'rel2.5'
def::parm tech.path '/rules/[def::parm -name tech.name]/[def::parm -name tech.version]'
def::parm tech.dips [list 
    sc gt hvt c16 latest 
    sc gt rvx c14 latest 
    sc gt lvt c16 latest 
    support cells latest 
    technology files latest 
    ]
def::parm pd.path [list . /projects/ChipX/incoming /projects/ChipX/pdl]
def::parm pd.power_nets [VDD VCS] 
def::parm pd.power_nets [VDD VCS VDD02 VDD03] design=TopLevel
dflow Design Analytics

- dflow gathers statistics for each step
  - store into a MySQL database

- Various utilities to “mine” the data
  - Progress/chart view for project managers and leads
  - Detailed statistics for engineers
Methodology Focus Areas

• First priority
  – Test
  – Clocking
  – Timing signoff

• Second priority
  – Floorplanning
  – Place and Route
### Test Advantages in FX-14™

<table>
<thead>
<tr>
<th>Design for Test Features</th>
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<tbody>
<tr>
<td>- DFT insertion with Industry-Standard Mux scan</td>
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<tr>
<td>- Robust DFT Verification and automated Test Pattern Generation performed by GF</td>
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<tr>
<td>- Physically-Aware Test Compression and scan insertion minimize layout impacts</td>
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<tr>
<td>- Out-of-Context DFT for re-use at all hierarchy levels</td>
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<td>- Hierarchical Test for partitioned test generation and testing</td>
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<td>- Partial Good Test for yield improvement</td>
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<th>Test Quality</th>
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<tr>
<td>- Competitive Fault Coverage ( &gt;99% stuck fault, &gt;85% at-speed)</td>
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<tr>
<td>- Transition Faults detected by At-Speed-Structural-Test (ASST)</td>
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<tr>
<td>- ASST utilizes both Launch off Capture (LOC) and Launch off Scan (LOS) for higher coverage</td>
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<tr>
<td>- On-Product clock generation allows for tests to be performed at functional speeds</td>
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<tr>
<td>- RAM Sequential Test (At-speed testing of Array Interfaces)</td>
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<tr>
<td>- IDDQ, voltage stress, min Vdd, Temp Sensitivity</td>
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<td>- Automated Diagnostics</td>
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<tr>
<td>- Automated DFT &amp; ATPG for embedded IP</td>
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<tr>
<td>- At-speed Memory BIST (RTL Insertion, Synthesis, Verification, and Pattern migration)</td>
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<tr>
<td>- Support for Advanced SerDes testing, including PRBS and Eye Quality verification</td>
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<tr>
<td>- Analog / Mixed Signal Test capabilities</td>
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<td>- IEEE 1687 Support for IP testing</td>
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<th>In-system Test Support</th>
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<td>- IEEE 1149.1 automation (Interconnect, Memory BIST, Optional internal access)</td>
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<tr>
<td>- IEEE 1149.6 automation (Advanced Interconnect)</td>
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Clocking

- Low skew for higher speed clocks
  - Structured Clock Buffer (SCB)
  - Drive SCB nets on highest layers
  - Traditional tree after 1-3 levels of SCB
  - Lowest variation, easier to close timing

- Traditional tree for lower speed clocks
  - Test clocks, other low speed functional clocks

- Useful skew
  - Limit to 50ps
  - Avoid in pre-CTS (for now)
Timing

• Transition from IBM statistical timing, but maintain competitive edge
  – Broad expertise in advanced nodes
  – Enable 2D interpolation (next page)
  – Enhanced waveform modeling

• Timing views
  – 4 timing views for pre-CTS
  – 20 timing views for CTS, post-CTS, post-route opt
  – 60 views for signoff

• On-the-fly view definition
  – Design team expects easy migration to latest inputs
    • Timing constraints – functional and DFT
    • Timing library versions
    • Operating conditions
  – dflow automatically replaces the database view information
Timing – interpolation

- Support for customer specific voltage and temperature conditions
- Tempus and Innovus support 2D interpolation
- Interpolation backed by Tempus to Spectre analysis
Floorplanning

• Bump creation and bump interconnect routing
• Macro-aware MIMCAP insertion
• Robust power routing
  – Flexibility to accommodate consumer designs
• IEEE-1801 (UPF) support
• Snapshot files (DEF)
  – Restore physical constraints for next iteration
  – Port assignment, macro placement, etc
Place and Route

• place_opt_design
  – Custom scan enable (SE) latch cloning for ASST timing
  – Scan XOR insertion for enhanced Test debug
  – Test mux attractions for improved timing
  – Pre-placed array Test logic for improved timing

• Signal Routing
  – NanoRoute modes tuned for FX-14™ with help from Cadence
  – routeDesign by default, can split as needed

• Custom Place and Route Checks
  – Additional checks to align with methodology/technology requirements
Managing the Innovus DB

• LEF / Lib links
  – Full link resolution locks in the DB during first init_design
  – Harder to upgrade when new IP arrives
  – Custom hook migrates to latest LEFs during restoreDesign

• Restore using –mmmcFile
  – Utilize on-the-fly view definition
  – Ensure the desired Lib/QRC are used, not the links in the DB

• Always write full DEF (except chip top)

• Extra files written into the DB
  – LEF for the block (used by parent)
  – NSE (non-standard extensions) for custom block properties (used by parent)
  – Tag information used by promotion (next slide)
Managing the Innovus DB (promotion/collection)

- Promote Innovus DBs to a central location
  - Many versions of all blocks and top level
- Collect a set of promoted DBs
  - No new data, just links
  - Easy for next step to pick-up (e.g., Timing)
- Utilizes DB “tags” to align with design analytics
  - Build analytical pedigree from a promoted DB
1. IBM ASIC
2. GF ASIC
3. GF ASIC Design Methodology
4. Tapeout Experiences
14nm Tapeouts

- Many customer tapeouts using GF 14LPP foundry process
- Several recent tapeouts using FX-14™
  - Innovus 15.15, Tempus 15.15
- Many in-flight designs using FX-14™
  - Innovus 15.22, Tempus 15.22
Block A

- 2.5M instances
  - 74 macros
- 500MHz, complex clocking
- Floorplan to post-route in 100 hours
  - 25h, place/pre-cts
  - 25h, cts
  - 15h, post-cts
  - 10h, routing
  - 25h, post-route
Challenges

• Growing pains
  – It’s all in the details

• Bleeding edge tools
  – Always using latest-and-greatest tool versions
  – Required many engineering builds
  – saveTestcase does not always reproduce the problem

• Concurrent Design/IP/Methodology development
  – Significant improvements from lessons learned on early designs

• Timing Closure
  – 60+ views versus 2-3 statistical runs in EinsTimer™
  – Getting to 100% done
  – Transition fails not fixed, out-of-bound fails, etc…
Successes

• Transition by GF ASIC team
  – New company, technology, tools, and methodology
  – Massive change in a short period of time
  – Cadence help was key to successful enablement

• Fast Prototyping
  – Ability to quickly run through routing for early feedback

• Runtime of construction flow
  – Improved place/opt/route runtime to lower TAT in RTx phases

• Cadence AE team
  – Worked nights/weekends to solve critical issues

• Cadence education
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2. GF ASIC
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Q & A