Fast Forward with In-design Pattern Matching and Fixing Flows

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GLOBALFOUNDRIES

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SNUG Silicon Valley
Agenda

GLOBALFOUNDRIES update
GLOBALFOUNDRIES reference flow
In-Design Signoff Pattern Matching Check
In-Design Auto-Fixing Pattern Matching repair (ADR)
Pattern Matching (PM) Library Runset and Fix Guidance
Results
Summary
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**Company Highlights**

<table>
<thead>
<tr>
<th>REVENUE</th>
<th>MORE THAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$~6B*</td>
<td>25,000</td>
</tr>
<tr>
<td></td>
<td>Patents &amp; Applications</td>
</tr>
<tr>
<td>2nd Largest Foundry</td>
<td>250 Customers</td>
</tr>
<tr>
<td></td>
<td>18,000 Employees</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FAB LOCATIONS</th>
<th>FAB CAPACITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burlington, East Fishkill, Malta, Dresden, Singapore</td>
<td>300mm Trusted Foundry</td>
</tr>
<tr>
<td>200K Wafers/Mo</td>
<td>200mm</td>
</tr>
<tr>
<td>133K Wafers/Mo</td>
<td></td>
</tr>
</tbody>
</table>

*Based upon analysts’ estimates
The First Truly Global Foundry

- East Fishkill, New York
- Malta, New York
- Burlington, Vermont
- Dresden, Germany
- Singapore

5 Manufacturing Centers on 3 Continents
Business Unit Structure

CMOS Platforms BU
Broad technology portfolio across Leading-Edge & Mainstream nodes

RF BU
Accelerating RF leadership and manufacturing scale
Differentiated RF portfolio solutions such as RF SOI, RF CMOS, and SiGe

ASIC BU
Richest portfolio of best-in-class IP for wired, wireless infrastructure applications in the foundry industry

Leveraging offerings across all BUs to provide solutions for Trusted, Aerospace, and Defense applications, spanning both government and commercial markets
Global Manufacturing Capacity
~7M Wafers / Yr*

<table>
<thead>
<tr>
<th>Location</th>
<th>Capacity in Wafers/Month</th>
</tr>
</thead>
<tbody>
<tr>
<td>East Fishkill, NY</td>
<td>14,000 (300mm)</td>
</tr>
<tr>
<td>Malta, NY</td>
<td>Up to 60,000 (300mm)</td>
</tr>
<tr>
<td>Burlington, VT</td>
<td>40,000 (200mm)</td>
</tr>
<tr>
<td>Dresden, Germany</td>
<td>60,000 (300mm)</td>
</tr>
<tr>
<td>Singapore</td>
<td>68,000 (300mm)</td>
</tr>
</tbody>
</table>

**TECHNOLOGY**

- 90nm–22nm
- 28nm, ≤ 14nm
- 350nm–90nm
- 45nm–22nm
- 180nm–40nm

*200mm Equivalents
Process Platforms

- Dynamic Body-bias
- Ultra-low Voltage Operation

14nm FinFET
- Performance/Power Efficiency
- Global Manufacturing

In Development

22nm FD-SOI

Mainstream Solutions
- High-volume Production
- Proven PPA

10/7nm

28nm

350 – 40nm
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GLOBALFOUNDRIES Reference Flow

- GLOBALFOUNDRIES DFM mandated tapeout sign-off requirements are well integrated into the design environment
  - **DRC+**: Litho hotspot detection and fixing
  - **DFM-POP**: Silicon-validated Pattern Optimization to enforce statistical yield improvement
- Yield layout enhancements cannot be done due to the large number of patterns to optimize
- Traditional approach of Litho hotspot fixing using rip-up and re-route
  - Requires several iterations and longer TAT for routing closure and sign-off
- DFM must be fast, integrated in the design and signoff flows, and provide automated fixing and optimization solutions
GLOBALFOUNDRIES Reference Flow

• GLOBALFOUNDRIES DFM-POP tool
  – Provides the framework to speed up the ECO
  – Enabling fixing guidelines in the pattern definition
  – Perform incremental DRC-clean pattern updates

• Synopsys ICV based auto fixing flow allows user-defined fixing guidance in the pattern library provided by the foundry
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Command Used

- **set_physical_signoff_options**
  - Set runset, layer map and exec_cmd (ICV)

- **signoff_drc**
  - Many Options available. Use as required
    - `signoff_drc -read_cel_view -max_errors_per_rule 1000 -user_defined_options {-turbo -D PM_1} -run_dir PM_run -unselect/select_rule {*PM.1*, *PM* }`
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Flow and Command Used

- **set_physical_signoff_options**
  - Set runset, layer map and exec_cmd (ICV)

- **signoff_autofix_drc**
  - Options available. Use as per your requirements. E.g.,
    - `signoff_autofix_drc -init_drc_error_db PM_run - config_file auto -max_errors_per_rule 1000 - user_defined_options { -turbo -D} - unselect/select_rule { *PM*, *PM.1*, *DPT*, }`
Flow:

- Identify matched patterns (hotspots) with ICV Pattern-Matching runset and reference pattern library.
- Enable Zroute to perform localized re-route for hotspot repair.
- Fixes have negligible timing impact due to localized scope of route fix.
In-Design Auto-Fixing Pattern Matching Results

Default Auto-Fix DRC:

<table>
<thead>
<tr>
<th>Rulename</th>
<th>TOTAL DRC</th>
<th>PROCESSED DRC</th>
<th>TARGETED DRC</th>
<th>REMAINING TARGETED DRC</th>
<th>FIX RATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM.Rule.C.1</td>
<td>129</td>
<td>129</td>
<td>129</td>
<td>24</td>
<td>-109/4</td>
</tr>
<tr>
<td>PM.Rule.C.2</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>6</td>
<td>-8/1</td>
</tr>
<tr>
<td>PM.Rule.C.3</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>9</td>
<td>-7/1</td>
</tr>
<tr>
<td>PM.Rule.C.4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>-2/0</td>
</tr>
<tr>
<td>PM.Rule.C.5</td>
<td>0</td>
<td>0</td>
<td>159</td>
<td>39</td>
<td></td>
</tr>
</tbody>
</table>

Average fixing rate of 60% achieved using default convergence

- Router does not change PG and clock net violations
- Router does not affect violation inside cell
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PM Library/Runset and Fix Guidance

(1) Prepare source hotspot patterns

- Source hotspot patterns are normally identified at a manufacturing site as know yield detractors.
- Some design companies also create their own patterns for methodology checking.
- Pattern layer(s) and marker layer are required.

(2) Write an executable ICV runset

```c
#include "icv.rh"

//User defined variables
//Layout database specifics
// General operations
//Layer assignment

//Define pattern library path
pattern_options(
    pattern_library_path = $PM_LIB_PATH);

//Create pattern library
pattern_learn(
    pattern_library_name = $PM_LIB_NAME,
    pattern_layers = {list of pattern layers},
    pattern_maker = pattern_maker,
    pattern_text_id = pattern_text_id,
    match_ambit = {0.2,0.2,0.2,0.2},
    ambit_mode = PM_MARKER_CENTER,
    pattern_fuzziness = PM_EDGE_UNIFORM,
    uniform_fuzzy_size = 0.004,
    edge_jog_size = 0.008,
    pattern_reflect = true,
    pattern_rotate = true);
```

(3) Run the job

```bash
%icv [command-line-options] runsetfile
```

- Pattern library stores in binary mode.
User-Defined Fixing Guidance

• ICV provides the functionality to specify user defined fix guidance
  - InsertWires and RemoveWires directives as part of MW router directives

• Order of applying the fixing guidance
  ✓ User-defined fixing guidance first
    ▪ ICC always starts with user-defined fixing guidance based on the order defined. If first guidance fails, next one will be applied
  ✓ Localized reroute second
Benefits of User-defined fixing guidance:

- Default ADR flow does localized re-route to fix PM hotspots
- Providing user-defined fixing guidance (add / subtract shapes) can do in-situ fixing
- Passed directly to the router through ICV `milkway_route_directives()`
- The user has better control over the automated pattern fixing flow
- Less repairing loops for faster convergence with much higher fixing rate
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Hotspot Repair with User-defined Fix Guidance
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<td>24 (-109</td>
<td>+4 )</td>
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<tr>
<td>PM.Rule.C.2</td>
<td>13</td>
<td>13</td>
<td>13</td>
<td>6 (-8</td>
<td>+1 )</td>
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<tr>
<td>PM.Rule.C.3</td>
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<td>15</td>
<td>15</td>
<td>9 (-7</td>
<td>+1 )</td>
</tr>
<tr>
<td>PM.Rule.C.4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>0 (-2</td>
<td>+0 )</td>
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<tr>
<td>PM.Rule.C.5</td>
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<td></td>
<td></td>
<td>159</td>
<td>75.5%</td>
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- Router does not change PG and clock net violations
- Router does not affect violation inside cell

Fix with user-defined Guidance:

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<td>0 (-129</td>
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• Good ADR fix rate has reduced manual fixing time and significantly improves overall project timeline

• Fix Guidance provided 100% fix rate in minimal repair loops

• All the fix and changes are performed on one database, maintains database integrity

• Pattern Matching runset is developed, qualified, maintained and released by GLOBALFOUNDRIES

In-Design Pattern fixing with guidance will save significant design cycle time
Questions & Answers
Thank You