Entering FD-SOI Era Using GLOBALFOUNDRIES 22FDX Technology

Ease of Design Combined with Tunable Performance/Power Optimization

Presenter: Tamer Ragheb
Authors: Stefan Block, Wolfgang Daub, Juergen Dirks, Farid Labib, Rainer Mann, Haritez Narisetty, Herbert Preuthen, Fulvio Pugliese, Tamer Ragheb, Richard Trihy

GLOBALFOUNDRIES

March 30-31, 2016
SNUG Silicon Valley
IoT/Sensor Market
Example: Remote Security Camera Application

22FDX Delivers:
- Optimization for Max performance and Minimal power
  - FBB for max performance
  - RBB for minimal power (low leakage and dynamic power)
- RF integration for reduced BOM cost

Integrated RF

Wakes up comms to transmit message

Wireless Comms

"Watchdog" Processor

Detects motion

Wakes up Image Processor to zoom in and analyze potential threat

22FDX die

FBB
22FDX Body-biasing
Power/Performance Trade-off

Leakage Power

Maximum Performance Operating Mode

Forward Body-bias (FBB)

Reverse Body-bias (RBB)

Minimum Leakage in Standby Mode

FBB and RBB are different devices

FDSOI: Fully Depleted Silicon-on-Insulator

-2V to +2V Body-Biasing

FBB and RBB are different devices

SLVT/LVT
- Lowest $V_T$
- Optimized for FBB
- Highest performance

RVT/HVT
- Mid-range $V_T$
- Optimized for RBB
- Balance of low leakage and high performance
Agenda

What is 22FDX Technology?
Body-Biasing: A New Dimension in Design Closure
Multi-Bias Domain Design Example
Implementation Details
Results
Conclusion
22FDX Technology

Bulk versus FDSOI

• What is 22FDX technology?
  – It is the new 22nm Fully Depleted Silicon-on-Insulator (FDSOI) technology from GLOBALFOUNDRIES

• Advantages:
  – Lower Leakage due to insulator layer
  – Enables Body Bias (BB) with minimal leakage impact
  – FDSOI variability is smaller across die due to lower doping effort

Effects of Body Biasing in Bulk Transistor and FDSOI Transistor
22FDX Technology

RBB versus FBB

• Bias voltage is applied to P-well and N-well

• Reverse Body Bias (RBB)
  – nMOS neg. substrate voltage, pMOS pos. substrate voltage
  – raising VT of these devices

• Forward Body Bias (FBB)
  – nMOS pos. substrate voltage, pMOS neg. substrate voltage
  – lowering VT of these devices
Agenda

What is 22FDX Technology?

Body-Biasing: A New Dimension in Design Closure

Multi-Bias Domain Design Example

Implementation Details

Results

Conclusion
22FDX Body-Biasing: A New Dimension in Design Closure

- Body-Biasing offers an additional option to tune cell performance or power:
  - Same implementation can be timed with different Bias voltages resulting in different performance results
  - Different Body-Biasing domains on one chip are enabling new design architectures and design styles

- PVT + BIAS $\rightarrow$ PVTB

- Recommend asymmetric BB (available in INVECAS libraries):
  - Reduction of 4X leakage (NWell is more leaky)
  - Performance is almost the same (more balanced)
22FDX Body-Biasing:
A New Dimension in Design Closure

- Static vs Dynamic Body-Biasing techniques:
  - Static: Need BB value optimization prior to implementation
  - Dynamic: Can use BB optimization on the spot after implementation
22FDX Body-Biasing: A New Dimension in Design Closure

- **Voltage map:** Additional entries for bias voltages at N-Well and P-Well

- **Power pins:** Additional pin definitions for N-Well and P-Well

```plaintext
pg_pin (VNW_N) {
    pg_type : nwell;
    physical_connection : device_layer;
    voltage_name : "VNW_N";
}
pg_pin (VPW_P) {
    pg_type : pwell;
    physical_connection : device_layer;
    voltage_name : "VPW_P";
}
```

```plaintext
voltage_map (VDD, XX);
voltage_map (VNW_N, 1);
voltage_map (VPW_P, -2);
voltage_map (VSS, 0);
```
Agenda

What is 22FDX Technology?

Body-Biasing: A New Dimension in Design Closure

Multi-Bias Domain Design Example

Implementation Details

Results

Conclusion
22FDX Multi-Bias Domain
Example Design - Specification

- Your RTL can be dissected into modules for better BB optimization:
  - Optimize modules rather than the whole design with module-specific BB
  - Avoid always-on synthesis
  - Does NOT require level shifters or isolation cells (same VDD) – Just spacing rule

<table>
<thead>
<tr>
<th>Module</th>
<th>VNW bias</th>
<th>VPW bias</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>OR1200_TOP</td>
<td>0V</td>
<td>0V</td>
<td>VDD(+/-10%)</td>
</tr>
<tr>
<td>OR1200_CPU</td>
<td>0V</td>
<td>-1V</td>
<td>VDD(+/-10%)</td>
</tr>
<tr>
<td>OR1200_DU</td>
<td>1V</td>
<td>-2V</td>
<td>VDD(+/-10%)</td>
</tr>
</tbody>
</table>
22FDX Multi-Bias Domain
Example Design - Floorplan

NET_BIAS0_VPW
NET_BIAS0_VNW

NET_BIAS1_VPW
NET_BIAS1_VNW

NET_BIAS2_VPW
NET_BIAS2_VNW

Common VDD and VSS for all 3 BIAS domains
$S =$ Spacing between BIAS areas
22FDX Multi-Bias Domain
Example Design – IEEE 1801-2009 – Key Bias Features

- Required by SNPS Tools:

```bash
set_design_attributes -elements {.} -attribute enable_bias true
```

- Create Supply Sets for each Bias Domain → Note that all three domains share same VDD/VSS:

```bash
create_supply_set ss_0
create_supply_set ss_1 -function {power ss_0.power} -function {ground ss_0.ground}
create_supply_set ss_2 -function {power ss_0.power} -function {ground ss_0.ground}
```

- Create Power Domain for each Bias Domain:

```bash
create_power_domain pd_bias_0
associate_supply_set ss_0 -handle pd_bias_0.primary

create_power_domain pd_bias_1 -elements {or1200_cpu}
associate_supply_set ss_1 -handle pd_bias_1.primary

create_power_domain pd_bias_2 -elements {or1200_du}
associate_supply_set ss_2 -handle pd_bias_2.primary
```
22FDX Multi-Bias Domain
Example Design – IEEE 1801-2009 – Key Bias Features (cont.)

• Define valid Power States for each Supply Set (only bias related shown):

<table>
<thead>
<tr>
<th>Supply Set</th>
<th>State</th>
<th>Supply Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>ss_0</td>
<td>no_bias_n_pd0</td>
<td>nwell == <code>\{FULL_ON, 0.0\}</code></td>
</tr>
<tr>
<td></td>
<td>no_bias_p_pd0</td>
<td>pwell == <code>\{FULL_ON, 0.0\}</code></td>
</tr>
<tr>
<td>ss_1</td>
<td>bias_n_1p0_pd1</td>
<td>nwell == <code>\{FULL_ON, 0.0\}</code></td>
</tr>
<tr>
<td></td>
<td>bias_p_m1p0_pd1</td>
<td>pwell == <code>\{FULL_ON, -1.0\}</code></td>
</tr>
<tr>
<td>ss_2</td>
<td>bias_n_2p0_pd2</td>
<td>nwell == <code>\{FULL_ON, 1.0\}</code></td>
</tr>
<tr>
<td></td>
<td>bias_p_m2p0_pd2</td>
<td>pwell == <code>\{FULL_ON, -2.0\}</code></td>
</tr>
</tbody>
</table>

• Define Supply Nets and Ports required for Layout:

<table>
<thead>
<tr>
<th>Supply Net</th>
<th>Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>NET_BIAS_0_VPW</td>
<td>NET_BIAS_0_VPW</td>
</tr>
</tbody>
</table>

• Bind Supply Sets to Supply Nets:

<table>
<thead>
<tr>
<th>Supply Set</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ss_0</td>
<td>{pwell NET_BIAS_0_VPW}</td>
</tr>
<tr>
<td></td>
<td>-update</td>
</tr>
<tr>
<td>ss_2</td>
<td>{nwell NET_BIAS_2_VNW}</td>
</tr>
<tr>
<td></td>
<td>-update</td>
</tr>
</tbody>
</table>
Agenda

What is 22FDX Technology?
Body-Biasing: A New Dimension in Design Closure
Multi-Bias Domain Design Example

Implementation Details
Results
Conclusion
22FDX Implementation Details

Tool Flow Overview

• Silicon-proven Synopsys Galaxy Platform
• Based on Multi-Voltage Aware Synopsys Reference Flow
• Coming soon:
  – IC Compiler II
  – IC Validator
22FDX Implementation Details
Library Preparation with Milkyway

• FRAM view has to be updated
  – To include Bias-Pins as PG-Pins

```
update_mw_port_by_db -bias_pg \
  -db_file GF22fdsoi_..._0P00V_0P00V_125C.db \
  -mw_lib GF22fdsoi.mwlib
```
22FDX Implementation Details

Synthesis with Design Compiler Graphical

- Multi-Voltage aware Synopsys Reference Flow
  - UPF includes supply set functions `pwell` and `nwell`
  - Synthesis is power domain aware → logical boundaries are preserved
  - Bias voltage levels are now part of the operating conditions
  - `set_voltage` commands are now extended

```
set_operating_conditions 0P72V_0P00V_0P00V_0P00V_M40C \
-library GF22fdsoi..._0P72V_0P00V_0P00V_0P00V_M40C.db \
-analysis_type on_chip_variation
```

```
set_voltage 0.72 -object_list ss_0.power
set_voltage 0.0  -object_list ss_0.ground
```

```
set_voltage 0.0  -object_list ss_0.nwell
set_voltage 0.0  -object_list ss_0.pwell
set_voltage 0.0  -object_list ss_1.nwell
set_voltage -1.0 -object_list ss_1.pwell
set_voltage 1.0  -object_list ss_2.nwell
set_voltage -2.0 -object_list ss_2.pwell
```
22FDX Implementation Details

Place & Route with ICC

• Based on Multi-Voltage aware Synopsys Reference Flow
  – UPF and bias-specific scenario settings same as for synthesis
    • UPF is important for validation as well, utilizing VC-LP
  – Floorplan includes
    • Additional physical cells to support Bias-Supply from external source
    • Voltage-Areas for each Bias-Domain
  – Power Planning includes Bias-Routes
  – Fill Insertion is Bias-Domain aware / VT aware
22FDX Implementation Details
Place & Route with ICC

• Based on Multi-Voltage aware Synopsys Reference Flow
  – CNRX (Continuous Diffusion) Placement
  – Special NDR Rules on Bias-Nets (HV rules)
    • Currently: assign proper NDR to each bias net to ensure correct spacing to the signal nets
    • Coming soon: automatically derive appropriate NDR from differential voltage of nets (bias net vs. signal net) and technology file (diff. voltage vs spacing) table

<table>
<thead>
<tr>
<th>Nominal Voltage</th>
<th>Signal Net Space</th>
<th>Bias Net Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>&gt;x1</td>
<td>&gt;y1</td>
</tr>
<tr>
<td>V2</td>
<td>&gt;x2</td>
<td>&gt;y2</td>
</tr>
<tr>
<td>V3</td>
<td>&gt;x3</td>
<td>&gt;y3</td>
</tr>
</tbody>
</table>
22FDX Implementation Details
Place & Route with ICC: Floor/Power-Planning

• Each Bias-Domain
  – Is a separate voltage_area
  – Must be enclosed with boundary cells
  – Must fulfill distance rules between its adjacent bias-domain
  – Contains Bias-Tap-Cells to supply wells with their respective bias voltage
  – Contains Bias-Strap-Pairs to supply the Bias-Tap-Cell with bias voltages
22FDX Implementation Details

Place & Route with ICC: Floor/Power-Planning

• Bias Tap-Cells
  – Supply N-Well and P-Well with Bias-Voltages from an external source
  – Are ideally placed in columns to minimize routing overhead due to additional Bias-Straps
  – Have to fulfill maximum distance rules between each other

• Bias-Routes
  – Provide Bias-Voltages to Bias-Tap-Cells
  – Can be connected to an on-die Bias-Voltage generator

[Diagram of bias tap-cells and bias routes with labels and labels such as NET_BIAS_2_VNW and METAL3-STRAP]
22FDX Implementation Details
Place & Route with ICC: Floor/Power-Planning

• Voltage Area
  – Min-distance rule

• Boundary Cells

• Tap-Cell Insertion
  – Per voltage area
  – Max-distance rules

• High Voltage Rules
  – Using NDR

```plaintext
create_voltage_area -power_domain pd_bias_2 -coordinate "X1 Y1 X2 Y2" -guard_band_x <val> -guard_band_y <val>

insert_boundary_cell -left_boundary_cell <left_edge_cell> \
  -bottom_left_outside_corner_cell <bottom_edge_cell>

add_tap_cell_array -voltage_area pd_bias_2 \
  -master_cell_name <external_bias_tapcell> \
  -well_port_name <VNW_N> -substrate_port_name <VPW_P> \
  -well_net_name "NET_BIAS_2_VNW" \ 
  -substrate_net_name "NET_BIAS_2_VPW" \ 
  -distance <tapcell_distance>

define_routing_rule MxVDD1V8_BIAS -default_reference_rule \ 
  -spacings {M1 XXX M2 XXX etc }
set_net_routing_rule -rule MxVDD1V8_BIAS \ 
  [get_flat_nets -all {NET_BIAS*}]```
22FDX Implementation Details
Place & Route with ICC: Floor/Power-Planning

• Bias Routes
  – Power plan strategies
  – Template based approach used: Auto-Align Straps over Tap-Cell Bias-Pins

```bash
set_power_plan_strategy -voltage_areas pd_bias_2 strategy_2 -nets NET_BIAS_2_VNW_N \
  -extension {{{nets: NET_BIAS_2_VNW_N} {direction: T} {stop: design_boundary}}}} \
  -template MyFDX.tpl:tapcell(<Layer>,<Width>,<Offset>,<TapCell>,<Pin>)

compile_power_plan -strategy strategy_2
```
22FDX Implementation Details
Place & Route with ICC: Filler Insertion

- Filler Insertion
  - Domain Aware
  - Mixed FBB-RBB special case: Execution per domain

```plaintext
insert_stdcell_filler -cell_without_metal <FBB-Fillers>
derive_pg_connect -reconnect

insert_stdcell_filler -voltage_area pd_bias_1 \ 
-cell_without_metal <FBB-Fillers> derive_pg_connect -reconnect

insert_stdcell_filler -voltage_area pd_bias_2 \ 
-cell_without_metal <RBB-Fillers> derive_pg_connect -reconnect
```
22FDX Implementation Details

Static Timing Analysis

- PrimeTime uses key features of the Multi-Voltage enabled flow
  - `load_upf or1200_top_routed.upf`
  - `set_voltage 0 -min 0 -object_list NET_BIAS_0_VNW_N`
  - Exact-Match library scaling group for each scenario:
    - Same Process
    - Same Temperature
    - Same VDD/VSS
    - Different Bias-Voltages

```bash
define_scaling_lib_group -exact_match_only \
{ GF22fdsoi...SS_0P72V_0P00V_0P00V_0P00V_125C.lib \ 
  GF22fdsoi...SS_0P72V_0P00V_0P00V_M1P00V_125C.lib \ 
  GF22fdsoi...SS_0P72V_0P00V_1P00V_M2P00V_125C.lib} 
```
Agenda

What is 22FDX Technology?
Body-Biasing: A New Dimension in Design Closure
Multi-Bias Domain Design Example
Implementation Details
Results
Conclusion
22FDX Results – OR1200 (FBB)

Using the Design Example

• Implementation @ Bias0 and Retiming @ Bias1 and @ Bias2
  – One implementation and 3 optimization points

• Impact of Bias vs Power vs Performance is shown:
  – Dynamic power increases linearly with frequency/performance increase
  – Leakage increase is more dramatic with body biasing
  – That is why total power increases from Bias1 to Bias2 much more than Bias0 to Bias1

• New feature: other bias point values can be interpolated by PrimeTime “BB Scaling”

![FBB Implementation Results Graph]

- VNW,VPW=0,0
- VNW,VPW=1V,-2V
- VNW,VPW=0,-1V
22FDX Results – OR1200 (RBB)

Using the Design Example

- Implementation @ Bias0 and Retiming @ Bias1 and @ Bias2
  - One implementation and 3 optimization points

- Impact of Bias vs Power vs Performance is shown:
  - Dynamic power decreases linearly with frequency/performance decrease
  - Leakage decrease is more dramatic with body biasing
  - That is why total power decrease behavior from Bias1 to Bias2 is different than Bias0 to Bias1

- New feature: other bias point values can be interpolated by PrimeTime “BB Scaling”
Conclusion

• Multi Bias Domain Implementation with GLOBALFOUNDRIES 22FDX is enabled in Synopsys tool flow
• Bias voltage control is a new dimension in power vs performance design tuning
• Bias voltage control enables new design architectures in the industry
  – Ex: RTL dissection optimization – Under development currently with Synopsys
• Design example is ready for download @GLOBALFOUNDRIES’ FoundryView

Tape-out proven Flow

GF Digital Design Reference Flow

Includes sample block tested at all RTL-to-GDS steps with Sign-off
Acknowledgement

- GLOBALFOUNDRIES Munich: The moving force behind this work
  - Wolfgang Daub
  - Herbert Preuthen
  - Farid Labib
  - Fulvio Pugliese
  - Stefan Block
  - Juergen Dirks

- GLOBALFOUNDRIES Dresden:
  - Rainer Mann

- GLOBALFOUNDRIES Santa Clara:
  - Tamer Ragheb
  - Richard Trihy
  - Haritez Narisetty

- Synopsys: Chris Zhou / Jens Peters / Michael Confal / Prabuddh Kumar / Josefina Hobbs / Zahra Karami
Thank You