Characterization and Variation Modeling for 22FDX™

Ning Jin
Digital Design Methodology Team
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Agenda

1. Introduction to 22FDX™ Technology
2. Library Characterization in Liberate and Variety
3. Library Characterization Qualification
4. Conclusion
22FDX™ Technology

Bulk versus FDSOI

• What is 22FDX™ technology?
  – It is the new 22nm Fully Depleted Silicon-on-Insulator (FDSOI) technology from GLOBALFOUNDRIES

• Advantages:
  – Lower Leakage due to insulator layer
  – Enables Body Bias (BB) with minimal leakage impact
  – FDSOI variability is smaller across die due to lower doping effort

Effects of Body Biasing in Bulk Transistor and FDSOI Transistor
Bias voltage is applied to P-well and N-well

Reverse Body Bias (RBB)
- nMOS neg. substrate voltage, pMOS pos. substrate voltage
- raising VT of these devices

Forward Body Bias (FBB)
- nMOS pos. substrate voltage, pMOS neg. substrate voltage
- lowering VT of these devices
22FDX™ Body Biasing

Power/Performance Trade-off

- Leakage Power
- Maximum Performance Operating Mode
- Forward Body-bias (FBB)
- Reverse Body-bias (RBB)
- Minimum Leakage in Standby Mode
- Max Frequency

FBB and RBB are different devices

FDSOI: Fully Depleted Silicon-on-Insulator

-2V to +2V Body-Biasing

FDSOI: Fully Depleted Silicon-on-Insulator

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22FDX™ Library Characterization

Body-Biasing Related Attributes

• Voltage map:
  – Supply voltages on N-Well and P-Well needs to be updated

• Power pins:
  – Pin definitions for N-Well and P-Well needs to be specified

• Body bias constructs added in power down function

```plaintext
voltage_map (VDD, XX);
voltage_map (VNW_N, 1);
voltage_map (VPW_P, -2);
voltage_map (VSS, 0);

pg_pin (VNW_N) {
  pg_type : nwell;
  physical_connection : device_layer;
  voltage_name : "VNW_N";
}

pg_pin (VPW_P) {
  pg_type : pwell;
  physical_connection : device_layer;
  voltage_name : "VPW_P";
}
```
Effect of Random Device Variability

• Delay variability (including CLK-to-Q delay)
  – The delay varies for each cell/edge (rise vs fall)/type (early vs late)
  – The delay varies based on the active arc/input transition/output load

<table>
<thead>
<tr>
<th>Cell</th>
<th>(min slew, min load)</th>
<th>(min slew, max load)</th>
<th>(mid slew, mid load)</th>
<th>(max slew, max load)</th>
<th>(max slew, min load)</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>1.22X</td>
<td>1.56X</td>
<td>1.0X</td>
<td>1.11X</td>
<td>6.78X</td>
</tr>
<tr>
<td>B</td>
<td>1.89X</td>
<td>1.33X</td>
<td>1.67X</td>
<td>1.44X</td>
<td>4.33X</td>
</tr>
<tr>
<td>C</td>
<td>1.44X</td>
<td>1.78X</td>
<td>1.22X</td>
<td>1.33X</td>
<td>2.58X</td>
</tr>
<tr>
<td>D</td>
<td>2.11X</td>
<td>1.67X</td>
<td>1.44X</td>
<td>1.44X</td>
<td>2.78X</td>
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• Constraints variability (Setup and Hold)
  – The constraints vary based on the slew on both Data_pin and CLK_pin

• Output transition
  – The output transition can vary with input transition and output load
Evolution of Design Margining Methodologies

- Different Design Margining Methodologies:
  - Global flat derate → On-Chip Variation (OCV)
  - Table based granular derates → Advanced OCV (AOCV)
  - Statistical approach → Statistical OCV (SOCV)
  - SOCV with slew/load dependency → Liberty Variation Format (LVF)

```plaintext
ocv_sigma_cell_rise (delay_template_7x7) {
    sigma_type : early;
    index_1 ("0.0020, 0.0050, 0.0100, 0.0190, ...");
    index_2 ("0.0005, 0.0015, 0.0040, 0.0100, ...");
    values ( "0.00136, 0.00138, 0.00146, 0.00160, 0.00178, ...");
    ...
    "0.0276, 0.0276, 0.0276, 0.0276, 0.0276, ...");
}

ocv_sigma_cell_rise (delay_template_7x7) {
    sigma_type : late;
    index_1 ("0.0020, 0.0050, 0.0100, 0.0190, ...");
    index_2 ("0.0005, 0.0015, 0.0040, 0.0100, ...");
    values ( "0.00136, 0.00138, 0.00144, 0.00160, 0.00178, ...");
    ...
    "0.02764, 0.02768, 0.02768, 0.02767, 0.02760, ...");
}
```

Pessimism Reduction

OCV
90nm and above

AOCV
65nm and below

SOCV/LVF
14nm and below

VARIATION in LVF
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Liberate Characterization Suite

- **Liberate™** enables characterization of advanced timing, and noise models (CCS, CCSN)

- **Variety™** enabling accurate on chip variation analysis and timing signoff with LVF modeling

- Complete characterization solution covering memories with **Liberate MX** and mixed signal blocks with **Liberate AMS**
Liberate Solution

Standard/custom cell characterization

• Foundation IP characterization
  - Full distribution per arc
  - Autonomous clients reduce network traffic, provide linear speed-up per CPU

• Multiple views
  - Liberty with CCS or ECSM for timing, noise, power
  - Verilog/Vital
  - Datasheet (html, pdf), custom API

• Fast and automated
  - Inside View approach to create vectors and function for digital cells
  - Re-characterize from existing library
  - Native API (SKI) integration with Spectre® simulator for 2-3X performance improvement over standalone SPICE
Variety

Process variation modeling

• Create SSTA, sigma variation tables for LVF libraries, or constraint margins (hold time)
  – Calculate delay sensitivity to global and local variation
  – Avoids costly Monte-Carlo runs
  – Fully distributed, multi-threaded

• AOCV/SOCV table generation
  – AOCV: User-controlled path length, interconnect, slew, load, fanout
  – SOCV: Tempus™ format, arc/slew/load/when dependent sigma factor in a side file

Enables reduced timing margins so you can tape out sooner with lower power!
Variety LVF

- Characterizes delay, slew and constraint sigmas for every input transition, output load and timing arc
  - Early and late sigmas are modeled separately
  - Each statistical parameter from variation mode is modeled independently
  - GLOBALFOUNDRIES technology models variation with 3 independent parameters

- Generates a “sensitivity file” which is a LVF format only .lib

- Sensitivity file can be read by Liberate™ and merged with a Liberate .db or an existing .lib
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Library Characterization Qualification

Experiment Setup

- Liberty file with NLDM + CCSTN data
- NLDM + CCSTN recharacterization in Liberate
- Implementation of ARM® Cortex®-A9 Processor Using baseline library
- Static Timing analysis in Tempus
  - Compare STA results against SPICE simulation to verify accuracy
Static timing analysis for 25 paths shows an average absolute difference of 0.51% against SPICE simulations.
Variation Characterization Qualification

Experiment setup

Liberty file with NLDM + CCSTN data

- Characterize LVF with MonteCarlo
- Characterize LVF using Sensitivity Base Analysis

- Compare LVF characterization runtime against NLDM+CCSTN
- Verify accuracy of sensitivity analysis against reference MonteCarlo

Implement ARM® Cortex®-A9 Processor

- Compare STA results against SPICE simulation to verify accuracy

Timing analysis in Tempus
Variation Characterization Qualification

Library Level Accuracy Evaluation Experiment

- Compare LVF accuracy from sensitivity based analysis and MonteCarlo simulations
- Based on the entire GLOBALFOUNDRIES 22FDX™ library cells

Library consisting of 102 cells
Reduced 2X2 input transition/output load tables are used

LVF Liberty File Using MonteCarlo

compare_library

LVF Liberty File Using sensitivity based analysis
Variation Characterization Qualification

Library Level Accuracy Evaluation Results – Delay sigma correlation

Delay sigma tolerance: 5%, 2ps
Pass rate: 98.74%
Average difference: 0.371ps
Average difference %: 0.55%
Variation Characterization Qualification

Library Level Accuracy Evaluation Results – Slew sigma correlation

Delay sigma tolerance: 5%, 2ps
Pass rate: 98.77%
Average difference: 0.349ps
Average difference %: 0.96%
Variation Characterization Qualification

Library Level Runtime Evaluation Experiment and Results

- Based on the entire GLOBALFOUNDRIES 22FDX™ library cells

Library consisting of 102 cells
Full 9X9 input transition/output load tables are used
3 independent process variation parameters

- NLDM/NLPM/CCST/CCS-Noise Library Generation
  - 50 CPUs
  - 1.63 hours

- Add-On Flow for LVF using Sensitivity Based Analysis
  - 1.31 hours

- < 1X runtime
Tempus Correlation Experiments
LVF Library Correlation Setup

Implementation of ARM® Cortex®-A9 Processor
Using baseline library

Static Timing Analysis in Tempus
Using baseline library with LVF add-on

SPICE MonteCarlo simulations (Golden Reference)
(μ+3σ) calculated for setup

Compare
Static timing analysis for 25 paths shows an average absolute difference of -1.30% against SPICE simulations.
Agenda

1. Introduction to 22FDX™ Technology
2. Library Characterization in Liberate and Variety
3. Library Characterization Solutions
4. Conclusion
Conclusion

• GLOBALFOUNDRIES 22FDX™ technology introduces body bias as an added characterization variable.

• Liberate library characterization tool models 22FDX™ libraries with necessary attributes and shows close correlation with SPICE simulations.

• Variety delay/slew variation characterization is qualified against SPICE and Monte Carlo.

• The runtime is fast with good balance of accuracy.
Next Step

• We are working on tightening hold variation correlation with MonteCarlo simulations in Variety.

• Setup variation characterization support using MC method came out recently in Variety. We will start testing out the new features and incorporate them into our flow.
Acknowledgement

GLOBALFOUNDRIES Design Methodology Team

Tamer Ragheb      Ramya Srinivasan      Sumanth Prakash
Thank you