AMS Design With GLOBALFOUNDRIES 22FDX™ Technology
Rais Huda
Agenda

1. Introduction to the 22FDX™ Technology
2. 22FDX™ Enablement
3. Test Chip Validated Methodologies and Guidelines
4. Conclusion
## Company Highlights

### Revenue

- ~$6B*<br/>

### More Than

- 25,000 Patents & Applications<br/>
- 250 Customers<br/>
- 18,000 Employees<br/>

### Fab Locations

- Burlington<br/>
- East Fishkill<br/>
- Malta<br/>
- Dresden<br/>
- Singapore

### Fab Capacity

- 300mm Trusted Foundry<br/>
- 200mm: 200K Wafers/Mo<br/>
- 200mm: 133K Wafers/Mo

*Based upon analysts’ estimates
Global Manufacturing Capacity: ~7M Wafers/Yr*

<table>
<thead>
<tr>
<th>Location</th>
<th>Technology</th>
<th>Capacity in Wafers/Month</th>
</tr>
</thead>
<tbody>
<tr>
<td>East Fishkill, New York</td>
<td>–</td>
<td>(300mm) Up to 60,000</td>
</tr>
<tr>
<td>Malta, New York</td>
<td>28nm, ≤ 14nm</td>
<td>(300mm) Up to 60,000</td>
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<tr>
<td>Burlington, Vermont</td>
<td>–</td>
<td>60,000 (300mm)</td>
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<tr>
<td>Dresden, Germany</td>
<td>45nm–22nm</td>
<td>68,000 (300mm)</td>
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<tr>
<td>Singapore</td>
<td>180nm–40nm</td>
<td>93,000 (200mm)</td>
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*200mm Equivalents
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The 22FDX™ Technology

- 22nm Fully Depleted Silicon on Insulator (FDSOI) Technology
- Architected for body bias capability

Conventional and flip well architecture (allowing forward and back body bias)

- Integrated RF

- Applications: IoT, wireless, wearables
Advantages of 22FDX™ Technology

- SOI => Lower leakage than bulk
- Fully depleted => Lower leakage
- Lower doping effort => Less variation across chip
- Body-biasing capability

![Advantages of 22FDX™ Technology](image-url)
Conventional vs Flip Well in 22FDX™

**Conventional Well**
- NMOS over P-well
- P-well biased 0 -> -2V
- PMOS over N-well
- N-well biased 0 -> +2V

**Flip Well**
- NMOS over N-well
- N-well biased 0 -> +2V
- PMOS over P-well
- P-well biased 0 -> -2V
Reverse Body Bias

- With conventional well devices
  - P-well biased 0 -> -2V
  - N-well biased 0 -> +2V
  - Back gate bias works “against” gate voltage
  - Effectively increases Vt
  - Ultra low leakage
Forward Body Bias

- With flip well devices
- N-well biased 0 -> +2V
- P-well biased 0 -> -2V
- Back gate bias "works with" gate voltage
- Effectively decreases Vt
- Ultra low voltage operation
- Increases performance
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The 22FDX™ AMS Flow

- Pre-Layout Functional Verification
- Accelerated Custom Layout
- MSOA Interoperability
- Physical Verification (Third Party Sign-Off Vendor)
- Parasitic Extraction & 3rd Party Vendor
- Post-Layout Functional Verification
- EM/IR
- DFM Module (Third Party Sign-Off Vendor)

- Cadence based flow
- Includes QRC and other 3rd party tool for extraction

- ADE-XL/MMSIM
- Schematic-XL/Layout-XL Layout-LDE Layout-EAD
- Virtuoso/EDI
- PVS
- QRC
- ADE-XL/MMSIM
- Voltus-Fi
22FDX™ Methodologies and Enablement

- BSIM-IMG Models (body-bias, self-heating etc)
- Body Biasing and Conventional/Flip/Tripl-Well handling
- Enhanced Pcells and FGRs
- PEX and EMIR QRC, Voltus-Fi
- Double Patterning ICADV12.2
- EAD, LDE kits
Need for Early Prediction of Parasitic Effects

Why EAD?
- More pronounced parasitics in smaller nodes
- Traditional designs flows require multiple iterations
  - Longer time to marked
  - Over design or margining

Using EAD
- Enables tracking of parasitic constraints and EM requirements during layout
- Enables simulation of parasitic effects while layout is being done
- Reduces design iterations
- Reduces over design or margining
EAD Flow in 22FDX™

EAD RC EMIR Design Aid

VSE XL
Create the design schematic

ADE XL/GXL
- Testbench setup
- Run simulation without parasitics
- Save current data from simulation results
- Resimulate
- Check design specs
- Optimize design

Process Technology File

Layout EAD
- Create layout
- Route nets
- Define geometric descriptions of nets
- Extract parasitics from nets
- Apply solver to calculate actual current through wires
- Load EM limits from technology files
- Perform EM checks by comparing computed currents

Is the computed current in limit?
- YES
- NO
More Layout Dependent Effects Increase Iterations and Development Time

- Custom LDE Engine extracts LDE device parameters from layout
- Virtuoso LDE allows LDE re-simulation with partial or non-LVS clean layout
- LDE Layout Analysis flags excessive shift between schematic and layout
- Detect early on device mismatch due to LDE
- Violations are automatically displayed in Virtuoso Annotation Browser and LDE Browser
- LDE Contribution and fixing guidelines accelerate root-cause analysis and reduces variation
Virtuoso LDE Flow has been Enabled in 22FDX™

- Extensive validation through 1000’s of validation structures
- Supports all Virtuoso LDE flow features
  - LDE-aware re-simulation
  - LDE-Matching constraints
  - LDE layout analysis
  - LDE contribution
  - LDE fixing guidelines
- Save design iterations
- Reduce over-design

Device: X_I_esgvtntfet_1_150_442_2000DUT_1
Device Type: esgvtntfet
Biasing Condition: vgs=0.8 vds=0.8 vbs=0.0

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<tr>
<td>vth</td>
<td>0.453</td>
<td>0.453</td>
<td>0%</td>
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LDE Engine Qualification
What is Double Patterning?

- Shape spacings are now so small that current light sources cannot print them reliably
- Solution is to split the dense shapes into two masks, each with more sparse shapes
- This process of splitting a single layer into two masks is called double patterning
- In 22FDX™, M1 and M2 are double patterned
Double Patterning Flow

- Decomposition Flow

  - Design with Colorless (and Optional Colored) Shapes
  - Oddcycle Clean?
  - Decomposition
  - Database with Fully Colored Shapes
  - Post-Decomp Verification
  - Submit Database to Foundry

- Fully Colored Flow
  - Customer does decomposition and submits fully colored layout
  - Customer has full control of color scheme
  - Customer needs to have proper methodology/planning for coloring requirements
  - Customer responsible for ensuring there are no color conflicts, no color balance issue etc
Double Patterning Requirements

- Requirements for Double Patterning
  - Odd-Cycle Clean
  - Same/Diff-Mask DRC Compliance

- Color density balance
Double Patterning with ICADV12.2

- Metal1 Color1/Mask1
- Metal1 Color2/Mask2
- Minimum Spacing Violation

Shapes with locked colors
Marker indicates a color conflict between shapes with locked colors
During editing, halos are displayed that show same mask and diff mask spacing
Requirements for IR drop and Electromigration Analysis

IR Drop

- Dynamic and static IR drop analysis
- Qualitative and quantitative analysis

EM Analysis

- Dynamic EM analysis
- IAVG, IRMS, IPEAK
  - Temperature and POH dependent
- LB Layer down to device contact
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Test Chip Validated Methodologies and Flows

- Developed specifically for flow/methodology validation
- Goals
  - Provide silicon proven flow and methodologies
  - Leverage the unique features of 22FDX™ to design analog benchmark circuits
  - Develop AMS design and layout guidelines
  - Prove out PDK quality and readiness

- Analog PLL
- Sigma-Delta ADC
- LC-VCO
- Regulated Charge Pumps (+/-)
- Current Steering DAC
- Opamps
22FDX™ Guidelines

- **Design Guidelines**
  - **Using FBB**
    - To create headroom for stacked devices by reducing $V_t$
    - To increase switching speeds (e.g. in dividers)
    - To control $g_m$
  - **Using RBB**
    - To reduce standby power
22FDX™ Guidelines

- Conventional/flip well layout
- Multi-voltage domains
- Device matching guidelines
- Layouts with deep nwells
- LDE Guidelines
22FDX™ Guidelines

- Double Patterning Guidelines
  - Recommended DPT flow
  - DPT layout best practices
  - Color-balancing techniques
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Summary

- The GLOBALFOUNDRIES 22FDX™ FDSOI technology provides high performance with low power and low cost.
- Key features required for designing with 22FDX™ are enabled in Cadence tool suites.
- AMS design methodologies, flows and guidelines for 22FDX™ available from GLOBALFOUNDRIES.
- Please contact your GLOBALFOUNDRIES representative for more details.
Acknowledgements

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Thank you