22FDX™ – Electrically Aware Design Methodology in GLOBALFOUNDRIES 22nm FDSOI Technology

Design Enablement Santa Clara: Rick Monga, Rajashekhar Chimalagi
Cadence EAD lead support: Sravasti Nair

3/24/2016
Agenda

• Introduction to GLOBALFOUNDRIES
• 22FDX™ Platform Features
• Conventional Design Flow
• EAD Value Proposition
• Techfile Generation and Execution
• EAD Flow Execution Setup
• EAD Browser Capabilities and Design Flow
• Results and Conclusion
## Company Highlights

<table>
<thead>
<tr>
<th>REVENUE</th>
<th>MORE THAN</th>
</tr>
</thead>
<tbody>
<tr>
<td>~6B*</td>
<td>250</td>
</tr>
<tr>
<td>$</td>
<td>Customers</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FAB LOCATIONS</th>
<th>FAB CAPACITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Burlington</td>
<td>300mm</td>
</tr>
<tr>
<td>East Fishkill</td>
<td>200K Wafers/Mo</td>
</tr>
<tr>
<td>Malta</td>
<td>200mm</td>
</tr>
<tr>
<td>Dresden</td>
<td>133K Wafers/Mo</td>
</tr>
<tr>
<td>Singapore</td>
<td></td>
</tr>
</tbody>
</table>

*Based upon analysts’ estimates*
Global Manufacturing Capacity: ~7M Wafers/Yr*

<table>
<thead>
<tr>
<th>Location</th>
<th>Technology Range</th>
<th>Capacity in Wafers/Month</th>
</tr>
</thead>
<tbody>
<tr>
<td>East Fishkill, New York</td>
<td>90nm–22nm</td>
<td>14,000 (300mm)</td>
</tr>
<tr>
<td>Malta, New York</td>
<td>28nm, ≤ 14nm</td>
<td>Up to 60,000 (300mm)</td>
</tr>
<tr>
<td>Burlington, Vermont</td>
<td>350nm–90nm</td>
<td>40,000 (200mm)</td>
</tr>
<tr>
<td>Dresden, Germany</td>
<td>45nm–22nm</td>
<td>60,000 (300mm)</td>
</tr>
<tr>
<td>Singapore</td>
<td>180nm–40nm</td>
<td>68,000 (300mm), 93,000 (200mm)</td>
</tr>
</tbody>
</table>

*200mm Equivalents
22FDX™ Platform Features

- Industry’s first 22nm fully-depleted silicon-on-insulator (FD-SOI) technology
- Delivers ultra-low power, FinFET-like performance at cost efficiency of 28nm planar
- Ultra-lower power consumption with 0.4 volt operation
- Software-controlled transistor body-biasing for flexible trade-off between performance and power
- Integrated RF for reduced system cost and back-gate feature to reduce RF power up to ~50%
- Enables applications across mobile, IoT and RF markets
EAD Value Proposition

• Conventional flow observations
  o Meeting timing constrains and resolving all violations for advanced nodes can often take several iterations
  o Extractions tools with older extraction techniques can introduce 25 to 100 percent error in this loop, making over-design and conservative timing necessary to offset inaccuracy
  o Overdesign can be expensive, resulting in higher power consumption, IR drop and electromigration risk, resulting in unnecessary timing closure iterations, increased noise, and coupling delay

• EAD Flow benefits
  o Modifying design at schematic stage by running simulations and keeping a tap on specifications
  o Analyze parasitic information for both partial and fully wired circuits
  o Dynamically extract parasitics and run EM checks as designs are being created
  o Compare results of an ideal simulation
  o Optimize design and verify the performance and reliability
EAD Flow Enabled in 22FDX™ PDK

- VXL or Layout
- GDS
- DEF
- OA
- Simulation (No parasitics)
- Schematic
- PVS
- Calibre
- PEX cmd options File
- IR/EMIR
- dyn power grid analysis fail
- dyn power grid analysis pass
- Log File
- DSPF
- SPEF
- SPICE
- Extracted View
- OA
- Simulation (with parasitics)

Simulation match

EAD RC EMIR Design Aid
22FDX™ EAD Flow

- VSE XL
  - Create the design schematic

- ADE XL/GXL
  - Testbench setup
  - Run simulation without parasitics
  - Save current data from simulation results
  - Resimulate
    - Check design specs
    - Optimize design

- Layout EAD
  - Create layout
  - Route nets
  - Define geometric descriptions of nets
  - Extract parasitics from nets
  - Apply solver to calculate actual current through wires
  - Load EM limits from technology files
  - Perform EM checks by comparing computed currents

Is the computed current in limit?

- YES
- NO

EAD RC EMIR Design Aid
Techfile Generation and Execution

• Tool versions
  o cadenceICADV/12.20.702 includes eadModelGen version 7.2.7r70
  o cadenceMMSIM/11.10.722 for adexl EAD flow testing

• RC eadTechFile creation
  o eadModelGen –protected_process -threads n -multi_cpu n
    22fdsoi_$BEOL_STACK_$corner_detailed.ict

• EMIR RC eadTechFile incremental update
  o eadModelGen –update_em
    cmos22fdsoi_$BEOL_STACK_T100_L11.4_CDF1e-9.emir.ict eadTechFile

• setup/22FDX.ini
  o connectivity, extraction, EM, display, extractionPrimitives, violationDisplay

• process/22FDX.ini
  o corners, EM, viaClustering, layerMapping, cellShapeTypes
EAD Flow Setup
EAD Browser Capability
EAD EMIR debugging using Browser Capability
EAD Testing setup using ADE-XL
EAD Adexl layout vs. schematic vs. extracted view – Simple Inverter
Simulation results for simple inverter layout/schematic

<table>
<thead>
<tr>
<th>Simulation</th>
<th>Falltime</th>
<th>Undershoot</th>
<th>Slew</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal Simulation</td>
<td>748.6</td>
<td>0.0932</td>
<td>1.44</td>
</tr>
<tr>
<td>EAD design aided flow post extraction</td>
<td>768.0</td>
<td>0.124</td>
<td>1.40</td>
</tr>
<tr>
<td>Conventional flow post extraction</td>
<td>762.1</td>
<td>0.162</td>
<td>1.39</td>
</tr>
</tbody>
</table>
Simulation results for hierarchical cascaded inverter layout/schematic
Simulation results for hierarchical cascaded inverter layout/schematic

<table>
<thead>
<tr>
<th>Simulation</th>
<th>Risetime</th>
<th>Overshoot</th>
<th>Slew</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal Simulation</td>
<td>1.352</td>
<td>0.136</td>
<td>796</td>
</tr>
<tr>
<td>EAD design aided flow post extraction</td>
<td>1.415</td>
<td>0.225</td>
<td>758</td>
</tr>
<tr>
<td>Conventional flow post extraction</td>
<td>1.415</td>
<td>0.225</td>
<td>758</td>
</tr>
</tbody>
</table>
Simulation results comparisons for Analog IP 22FDX V0.4_1 EAD flow

EAD and pex extracted view

Ideal Simulation
Conclusions

• EAD Flow Benefits
  o Cuts down design cycle time that provides results on partial designs for design awareness
  o Dynamically extract parasitics and run EM checks
  o Compare results of an ideal simulation to various stages in design
  o Optimize design and verify the performance and reliability

22FDX™ - Industry first FD-SOI Technology with FinFet like performance enables designers to leverage these benefits by supporting EAD in the Design Flow